US009478545B2

(12) **United States Patent**
Masuoka et al.

(10) **Patent No.: US 9,478,545 B2**
(45) **Date of Patent: *Oct. 25, 2016**

(54) METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **14/963,432**

(22) Filed: **Dec. 9, 2015**

(65) **Prior Publication Data**

US 2016/0111427 A1 Apr. 21, 2016

Related U.S. Application Data

(63) Continuation of application No. 14/537,322, filed on Nov. 10, 2014, now Pat. No. 9,245,889, which is a continuation of application No. 14/066,095, filed on Oct. 29, 2013, now Pat. No. 8,916,478, which is a

(Continued)

(51) **Int. Cl.**
H01L 27/01 (2006.01)
H01L 27/12 (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC ***H01L 27/0924*** (2013.01); ***H01L 29/0653*** (2013.01); ***H01L 29/1037*** (2013.01);
(Continued)

(58) **Field of Classification Search**
CPC H01L 21/8238; H01L 21/845; H01L 21/823487; H01L 27/0924; H01L 27/0251; H01L 27/0886; H01L 27/1104; H01L 29/0852; H01L 29/66666; H01L 29/7827
USPC 257/350, 359, 384, 358, 367, 328, 788, 257/E21.006, E21.007, E21.014, E21.042, 257/E21.043, E21.048, E21.051, E21.151, 257/E21.165, E21.173, E21.278, E21.293, 257/E21.288
See application file for complete search history.

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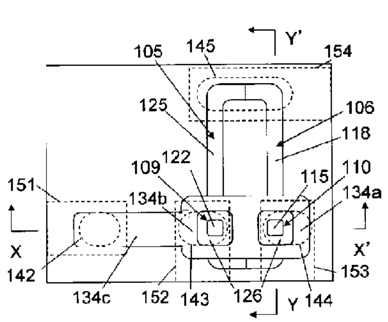
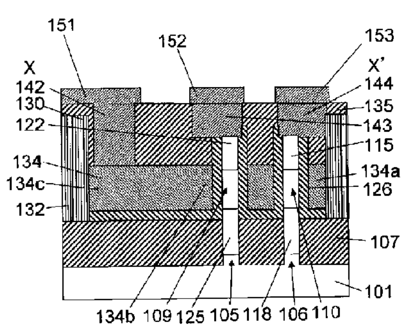
(57) **ABSTRACT**

A semiconductor device includes a first and second fin-shaped semiconductor layers on a substrate. A first insulating film is around the first and second fin-shaped layers. A first and second pillar-shaped semiconductor layers reside on the first and second fin-shaped layers, respectively. A width of a bottom of the first pillar-shaped semiconductor layer is equal to a width of a top of the first fin-shaped semiconductor layer, and a width of a bottom of the second pillar-shaped semiconductor layer is equal to the width of a top of the second fin-shaped semiconductor layer. First and second gate insulating films and first and second metal gate electrodes reside around the first and second pillar-shaped layers, respectively. A metal gate line is connected to the first and second metal gate electrodes and extends in a direction perpendicular to the first and second fin-shaped layers.

1 Claim, 52 Drawing Sheets





Related U.S. Application Data

continuation-in-part of application No. 13/693,524, filed on Dec. 4, 2012, now Pat. No. 8,772,175.

(60) Provisional application No. 61/577,189, filed on Dec. 19, 2011.

(51) **Int. Cl.**

H01L 31/0392	(2006.01)
H01L 27/092	(2006.01)
H01L 29/78	(2006.01)
H01L 29/66	(2006.01)
H01L 29/423	(2006.01)
H01L 29/06	(2006.01)
H01L 29/10	(2006.01)

(52) **U.S. Cl.**

CPC ... ***H01L29/42392*** (2013.01); ***H01L 29/66545*** (2013.01); ***H01L 29/66666*** (2013.01); ***H01L 29/7827*** (2013.01)

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FIG. 1A

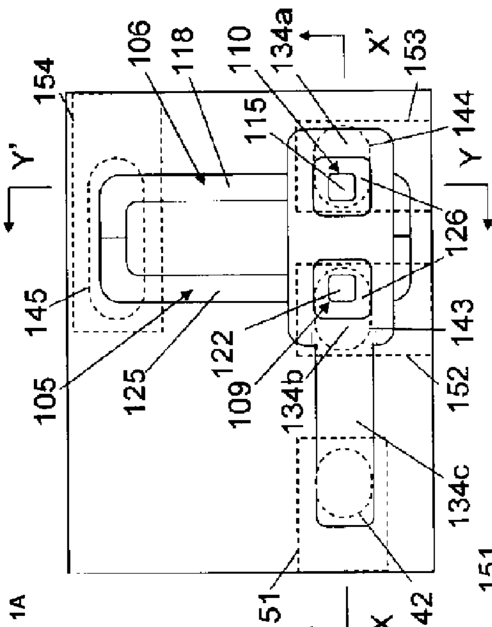


FIG. 1B

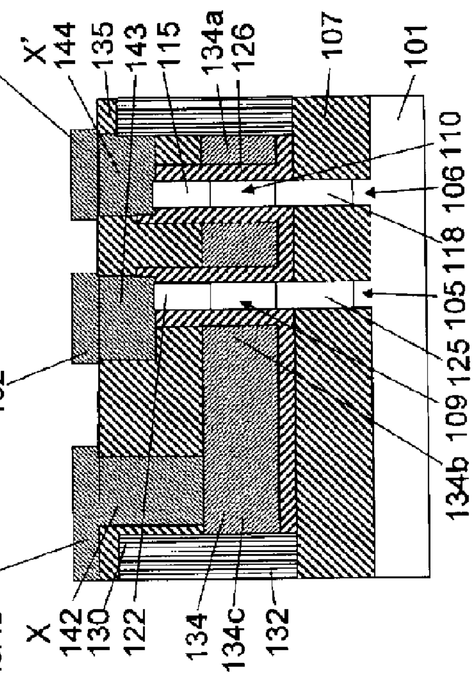
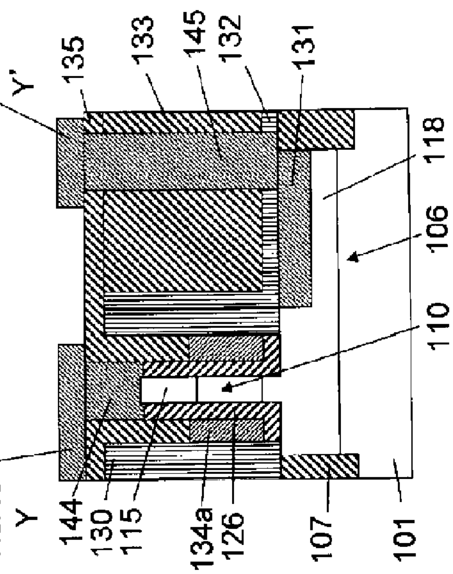


FIG. 1C



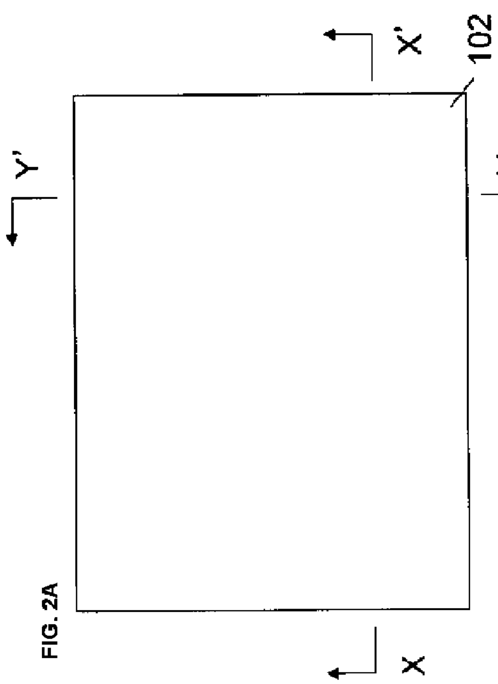


FIG. 2A

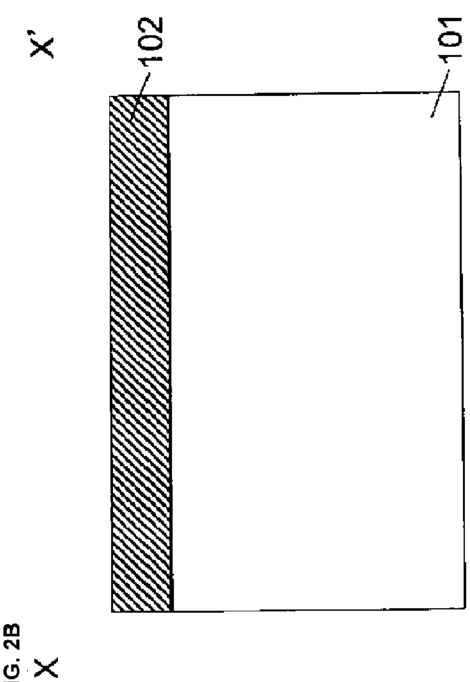


FIG. 2B

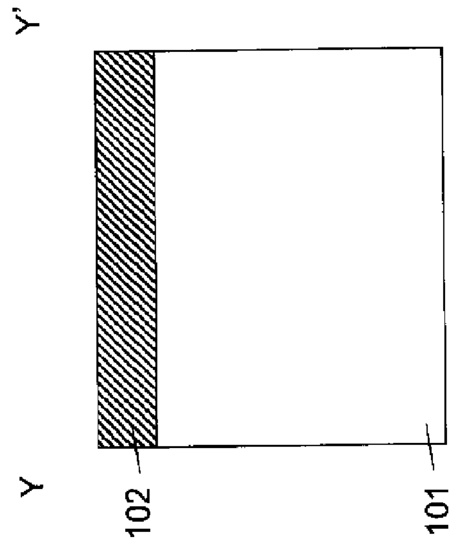


FIG. 2C

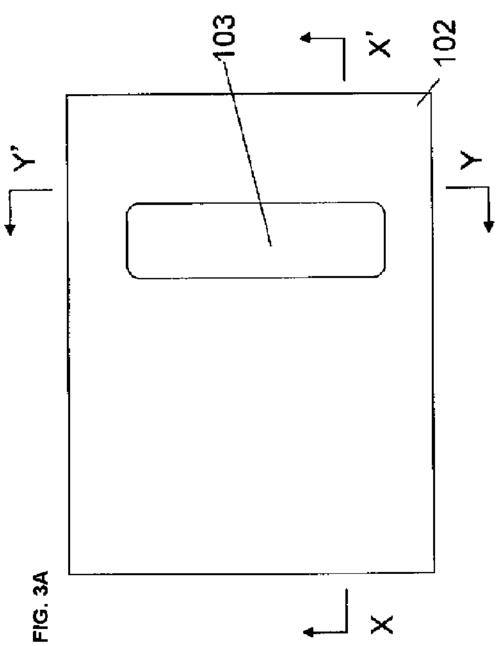


FIG. 3A

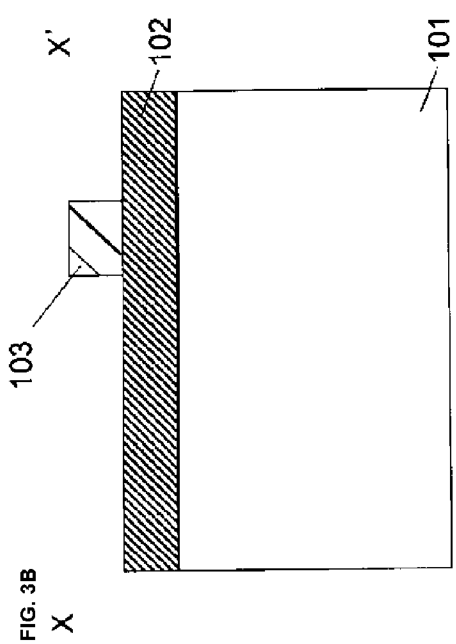


FIG. 3B

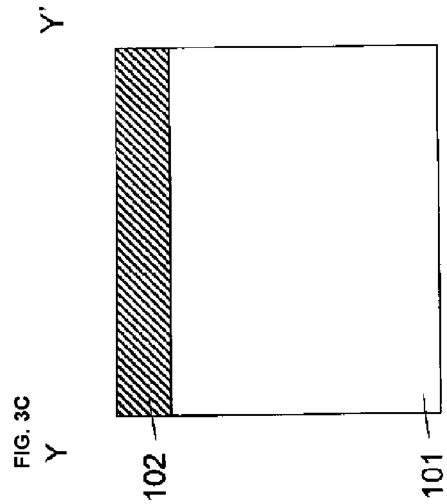


FIG. 3C

FIG. 4A

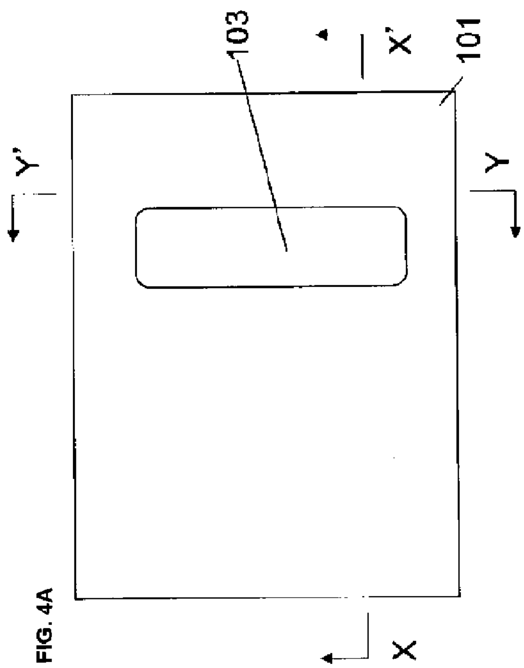


FIG. 4B

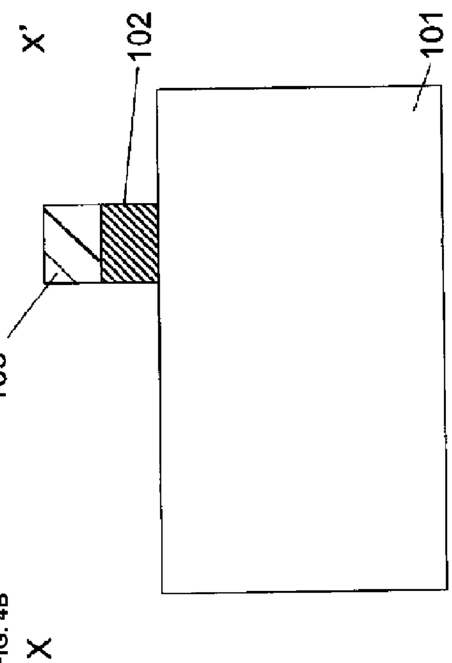


FIG. 4C

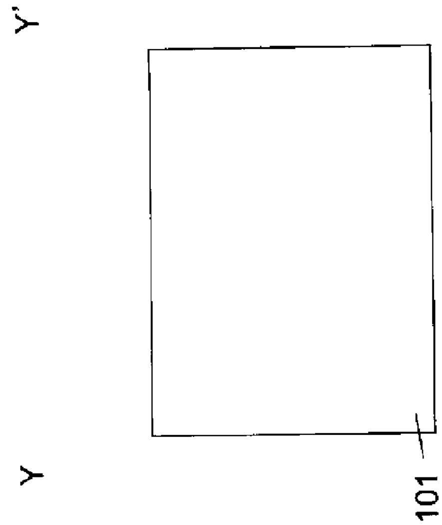


FIG. 5A

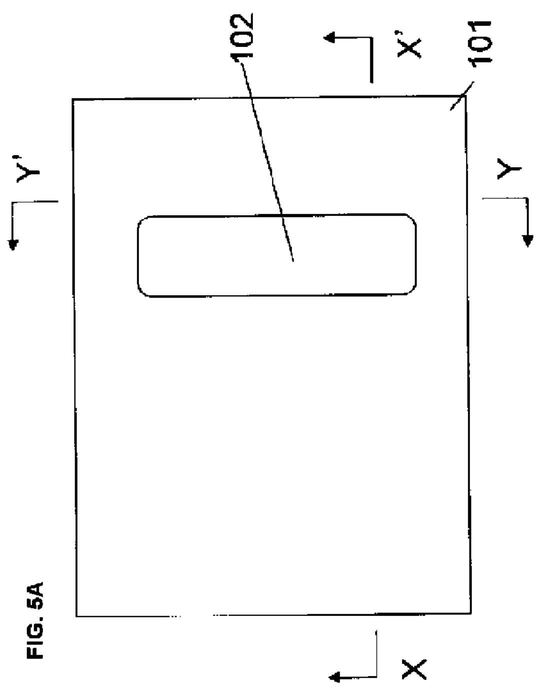


FIG. 5B

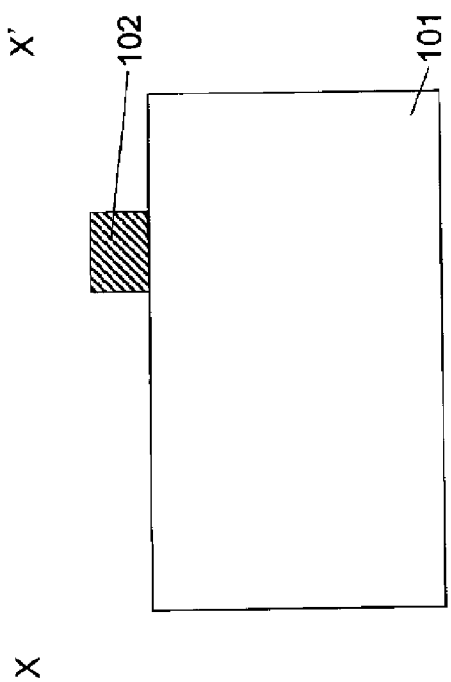
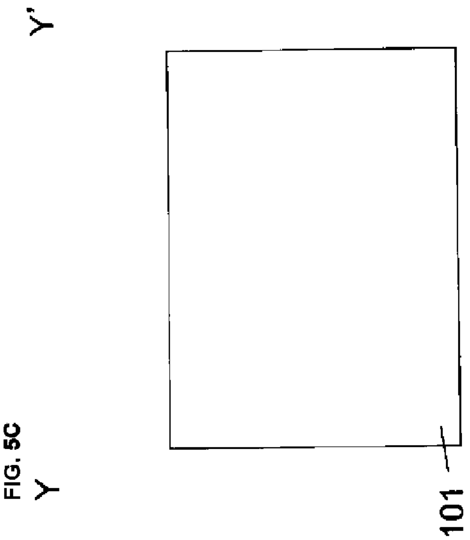


FIG. 5C



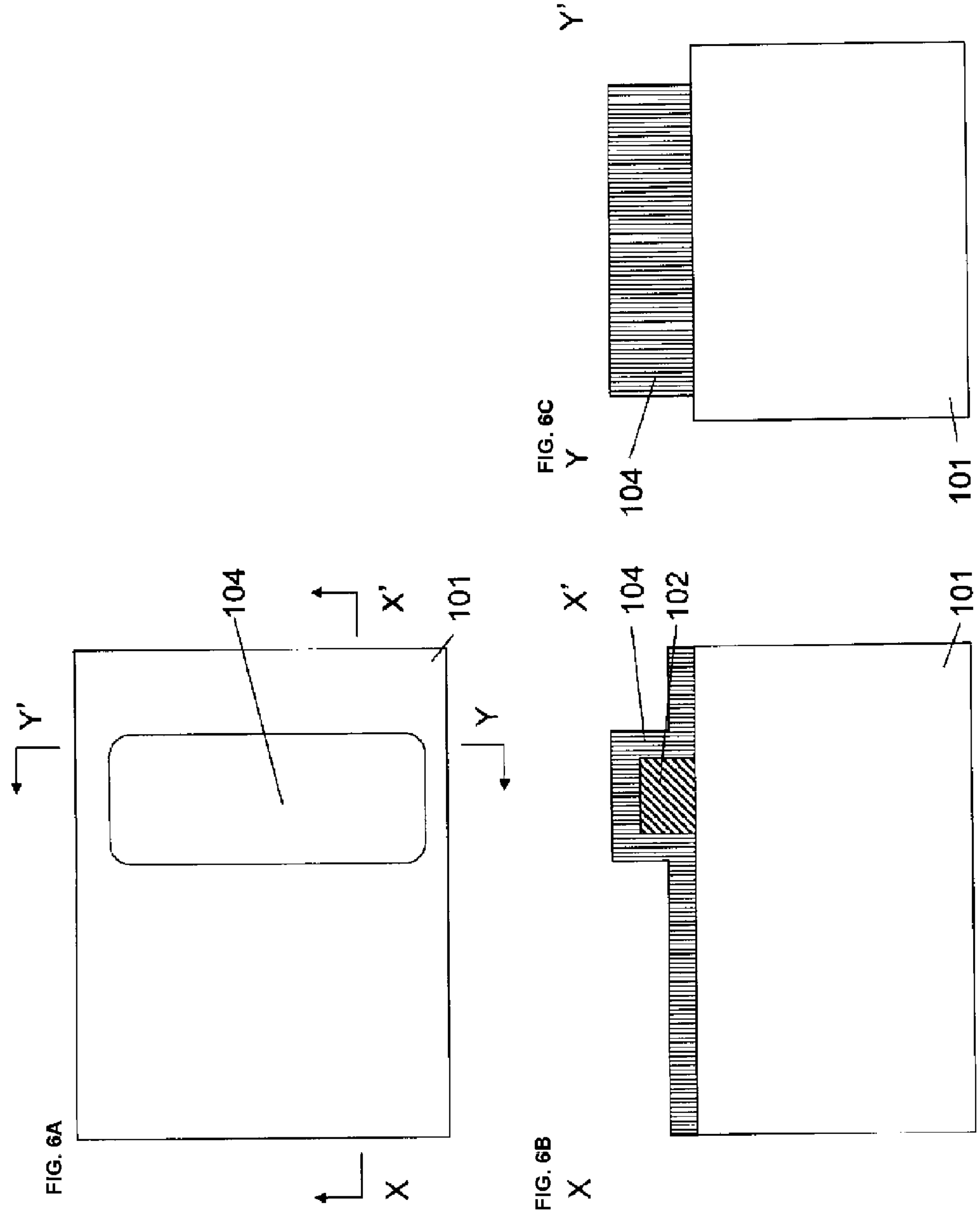


FIG. 6A
FIG. 6B
FIG. 6C
X
X'
Y
Y'
101
102
104

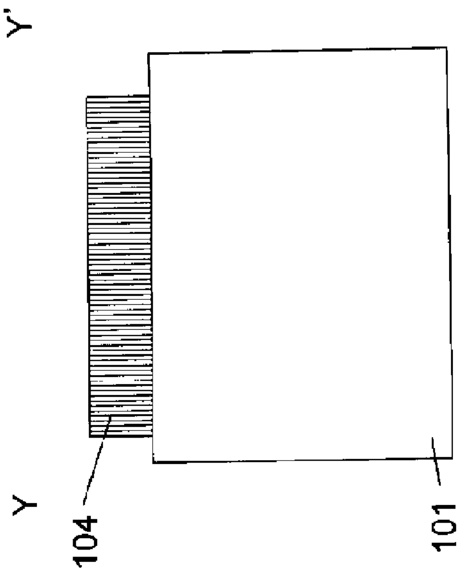


FIG. 7C

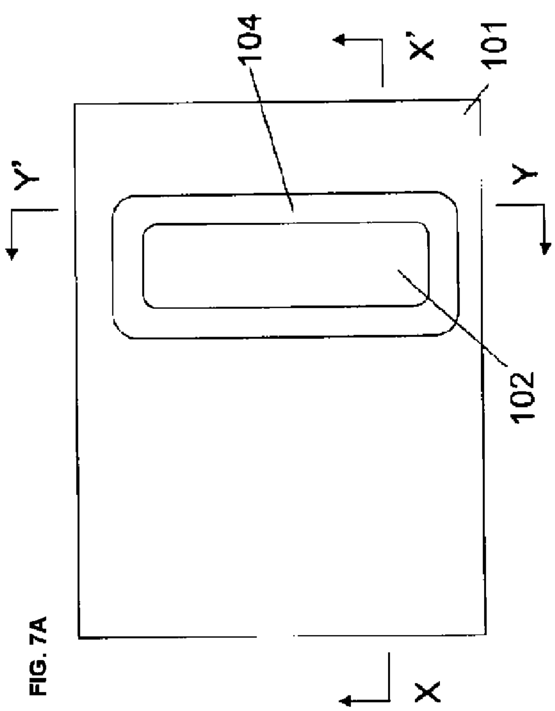


FIG. 7A

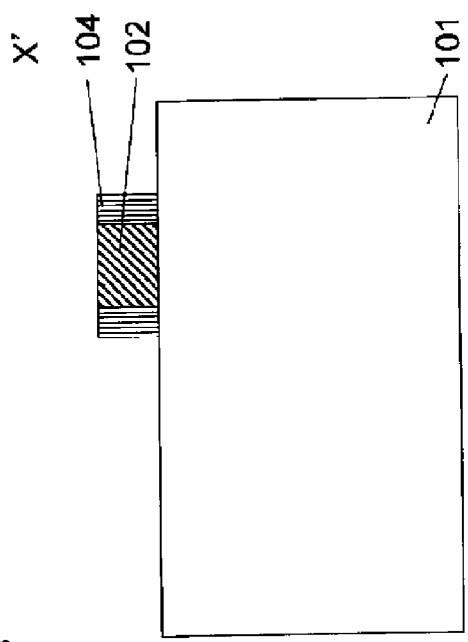


FIG. 7B

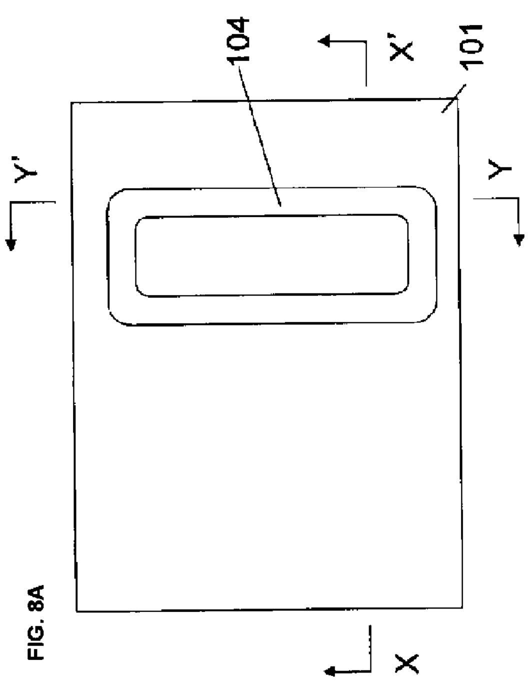


FIG. 8A

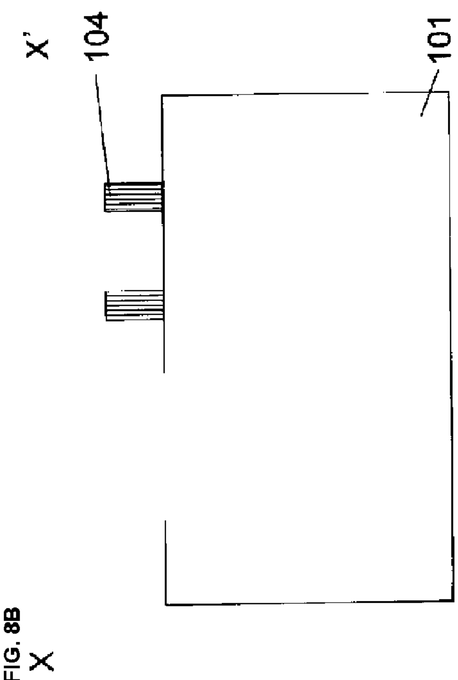


FIG. 8B

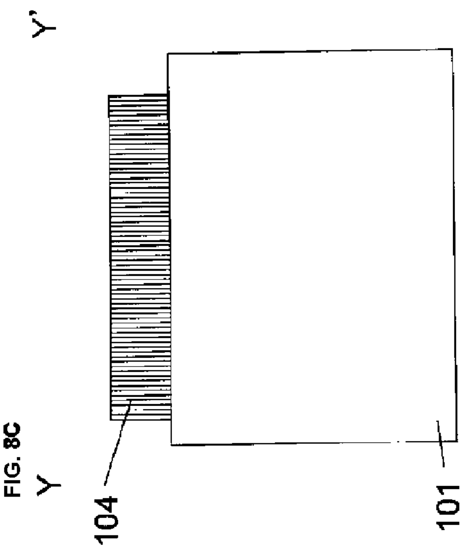


FIG. 8C

FIG. 9A

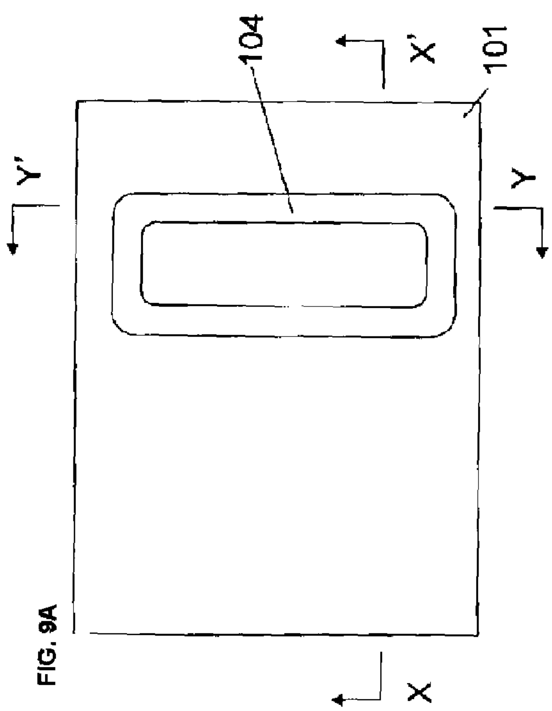


FIG. 9B

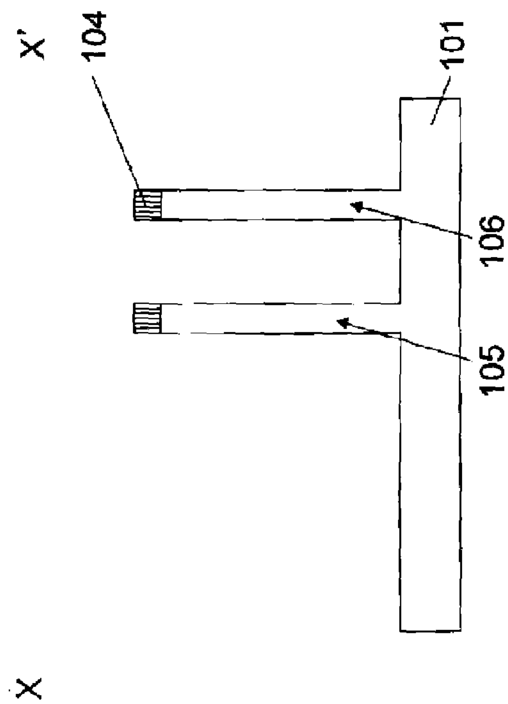
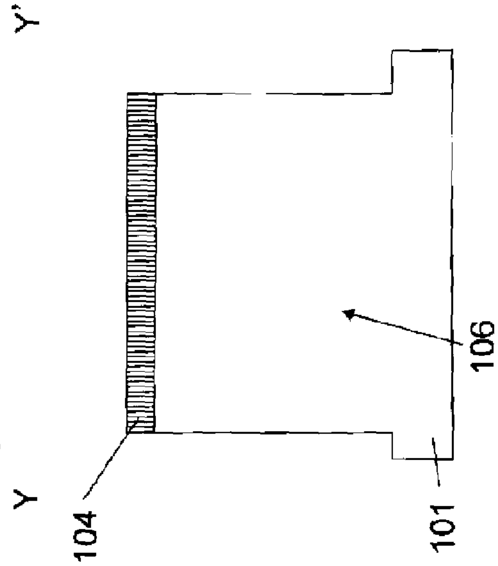


FIG. 9C



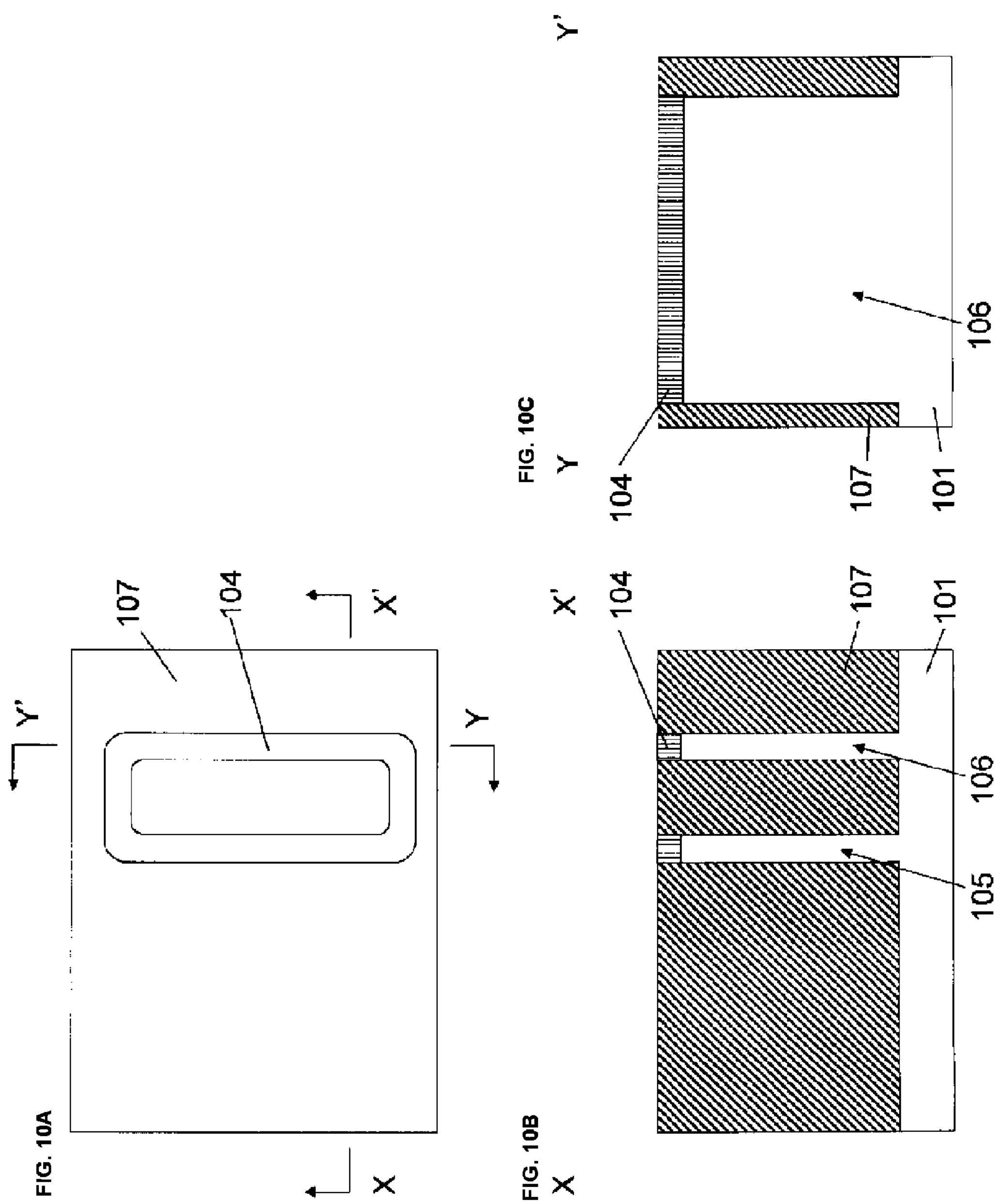


FIG. 10A

FIG. 10B

FIG. 10C

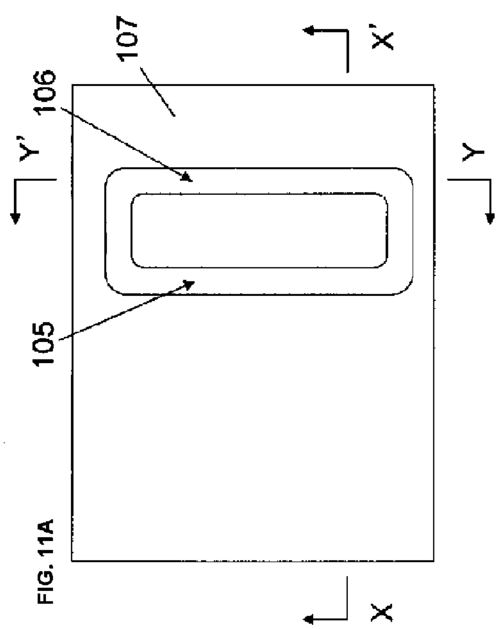


FIG. 11A

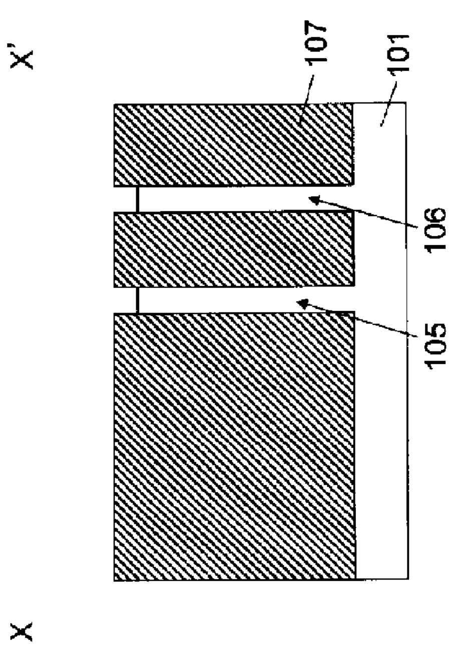


FIG. 11B

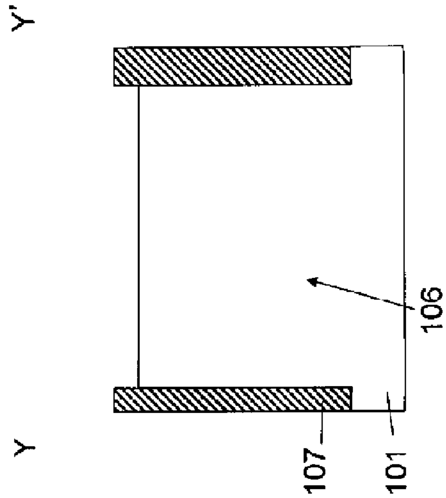


FIG. 11C

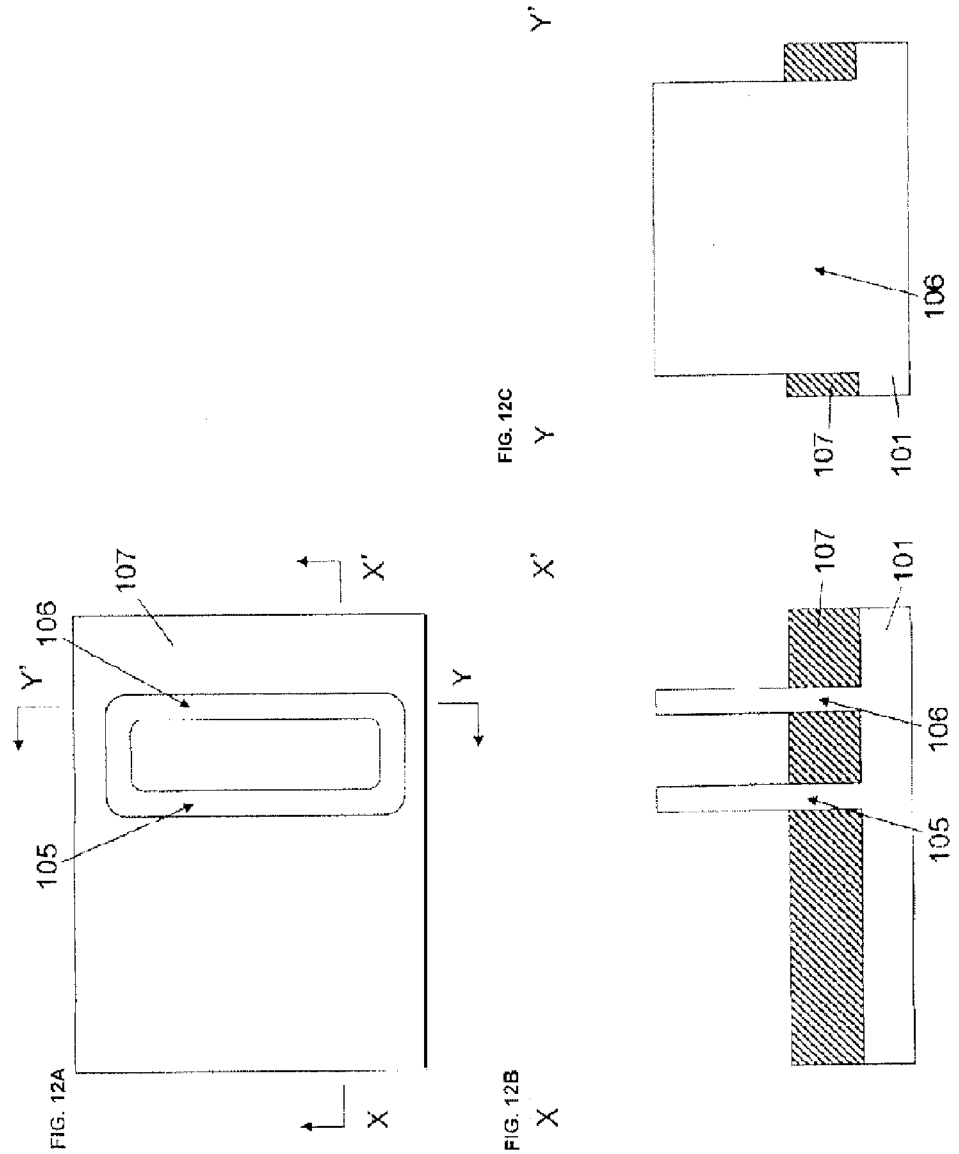


FIG. 12A

FIG. 12B

FIG. 12C

FIG. 13A

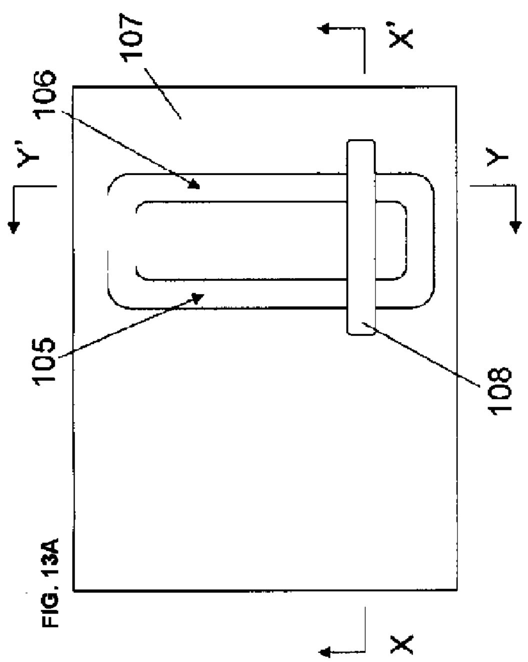


FIG. 13B

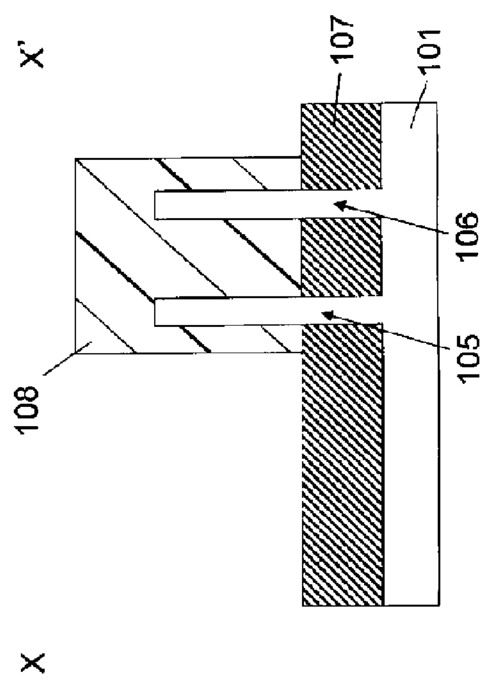
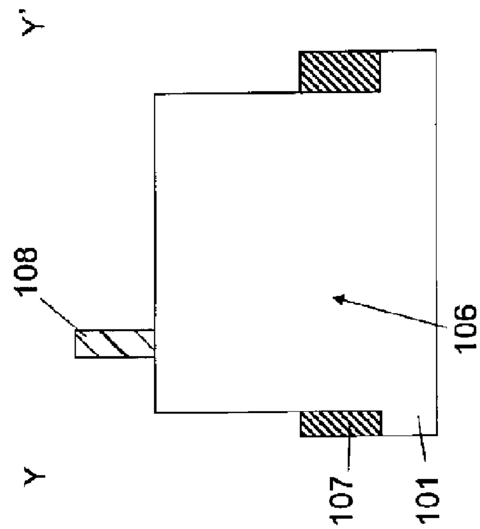


FIG. 13C



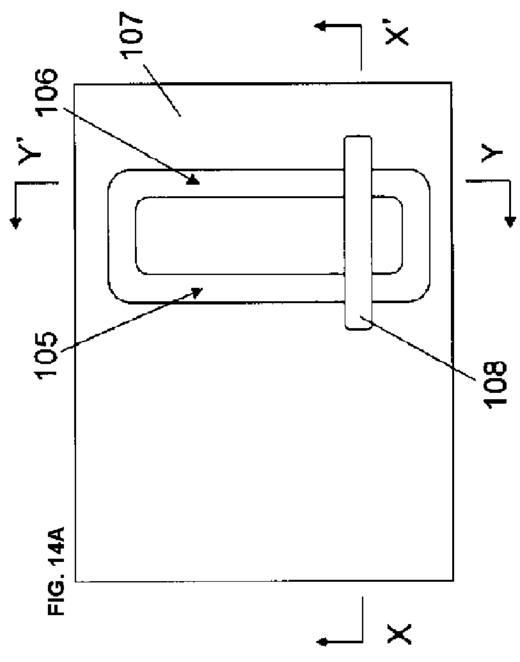


FIG. 14A

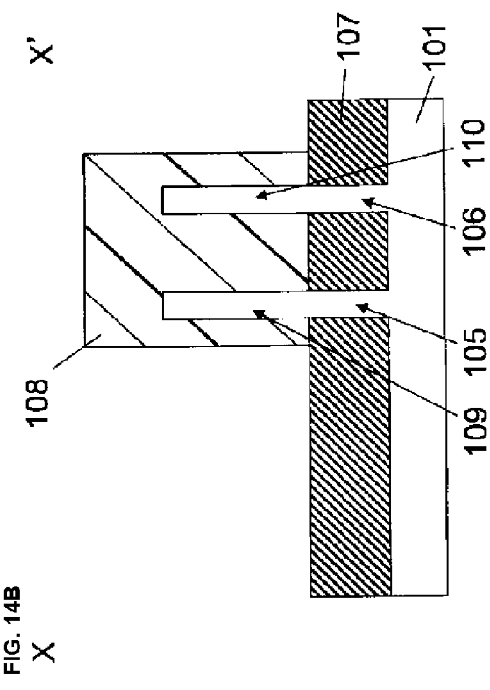


FIG. 14B

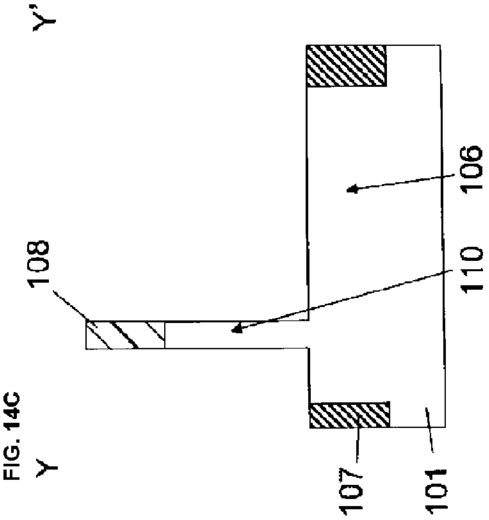


FIG. 14C

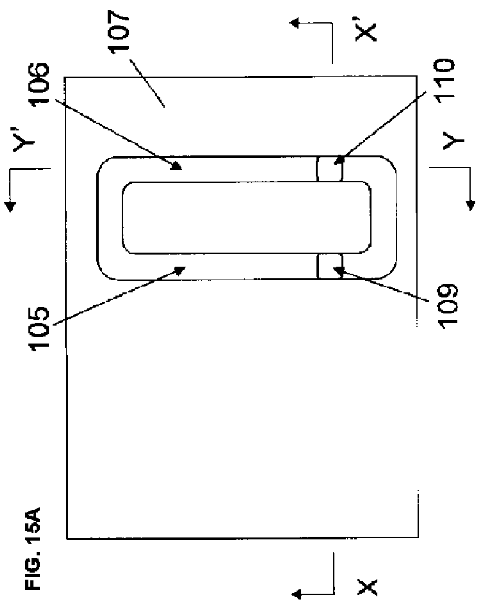


FIG. 15A

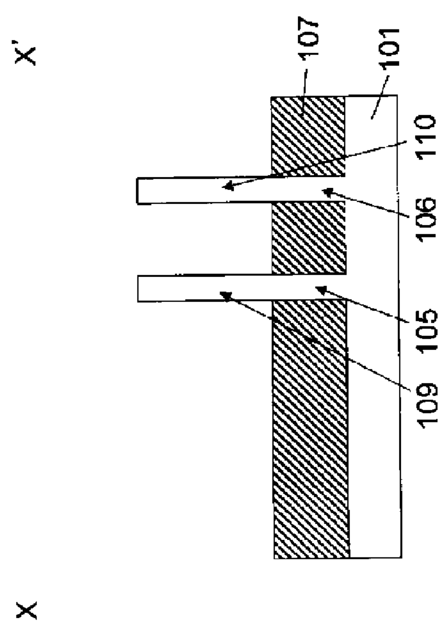


FIG. 15B

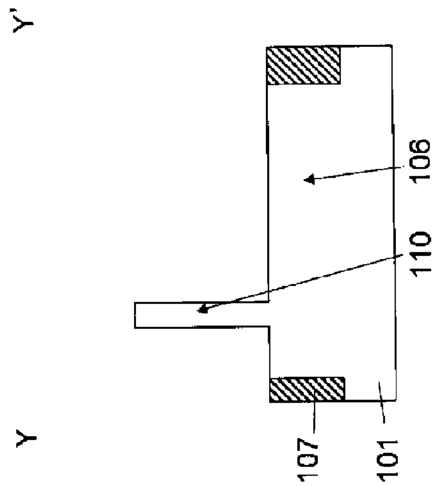


FIG. 15C

FIG. 16A

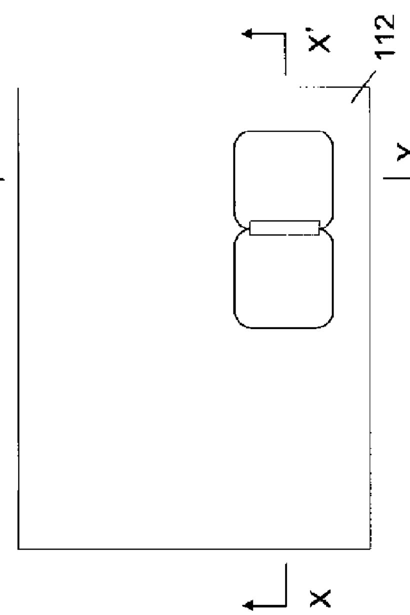


FIG. 16B

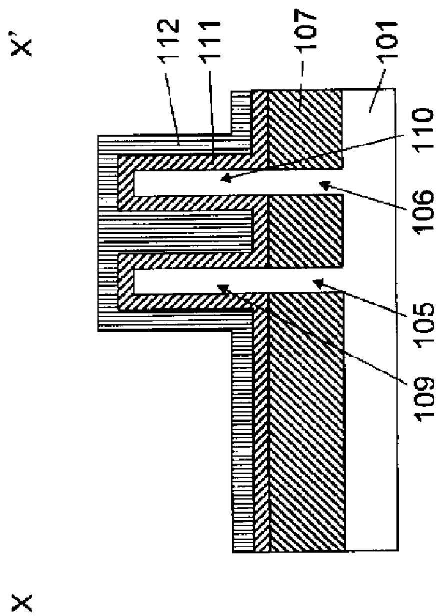


FIG. 16C

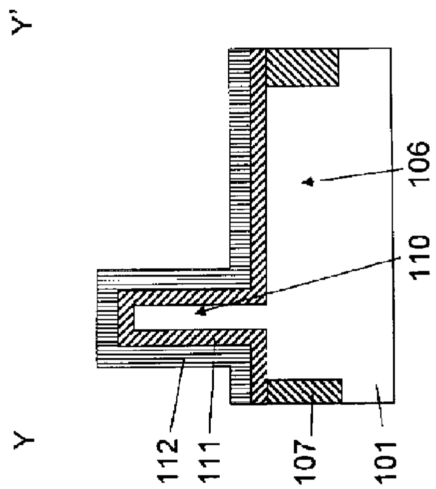


FIG. 17A

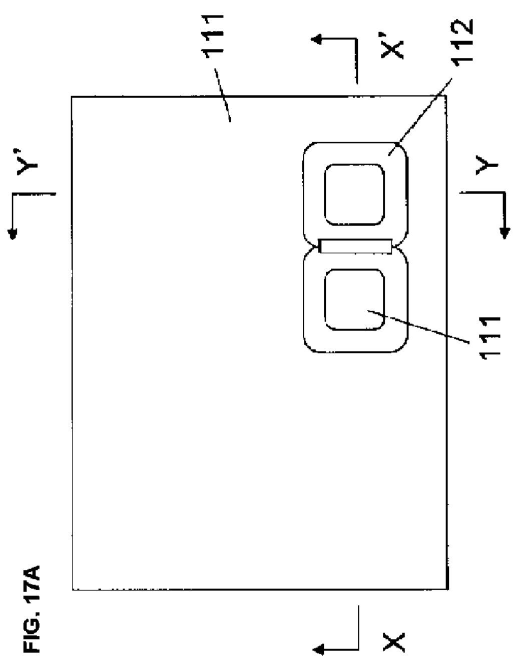


FIG. 17B

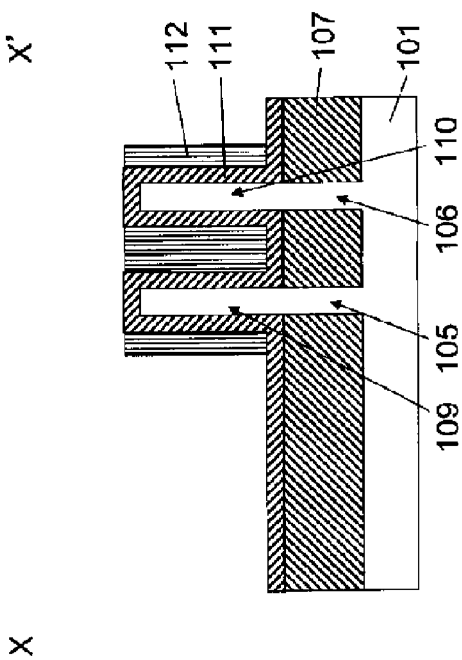


FIG. 17C

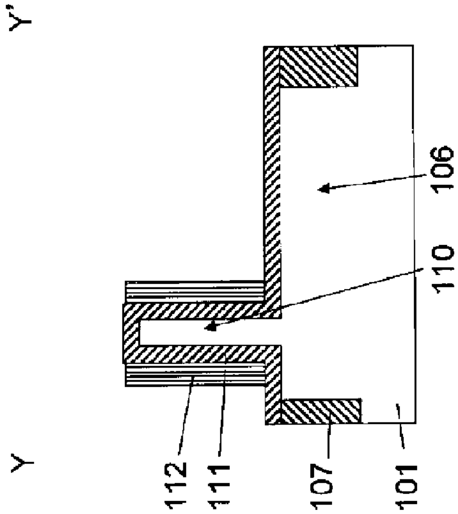


FIG. 18A

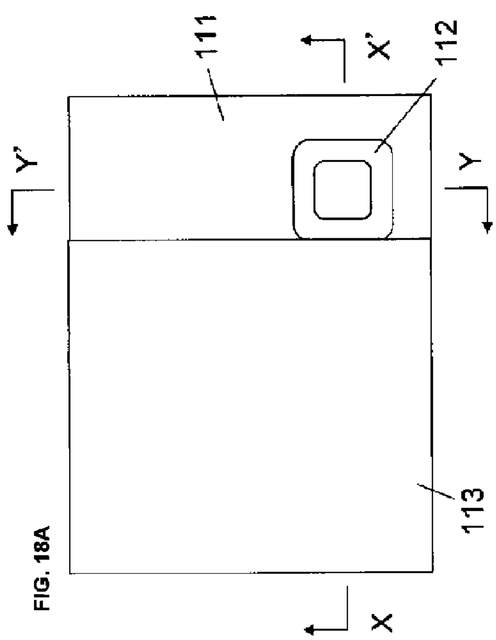


FIG. 18B

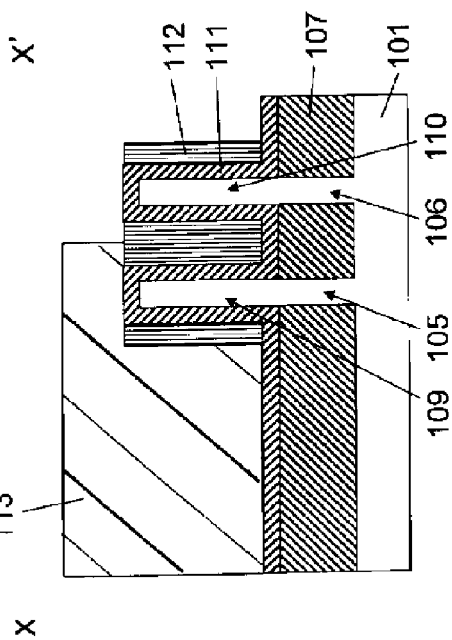


FIG. 18C

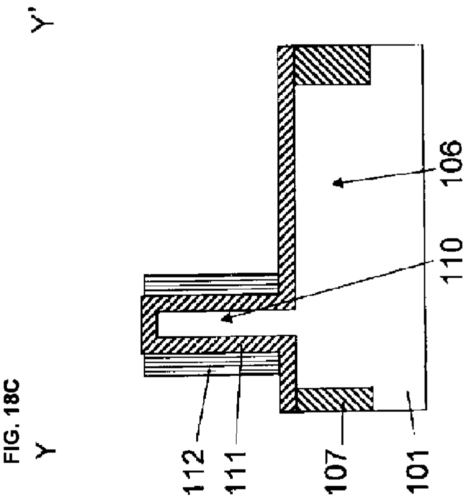


FIG. 19C

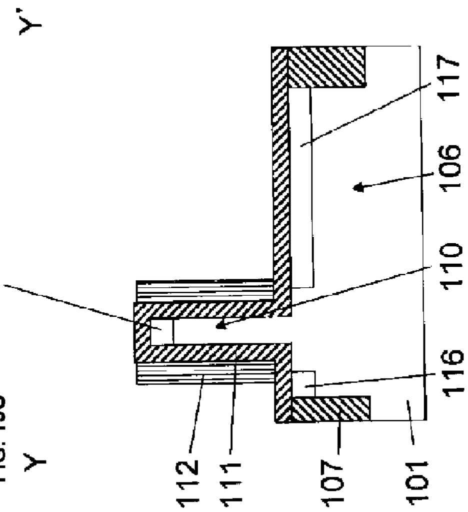


FIG. 19A

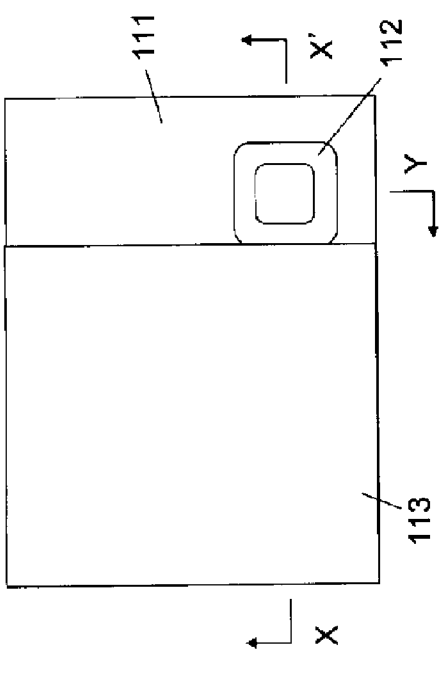
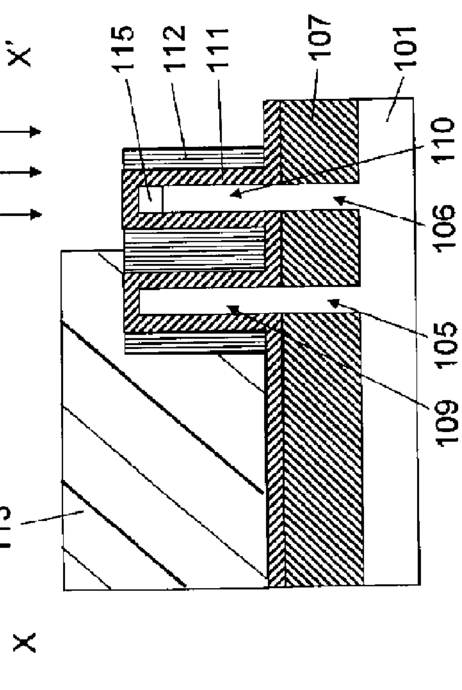


FIG. 19B



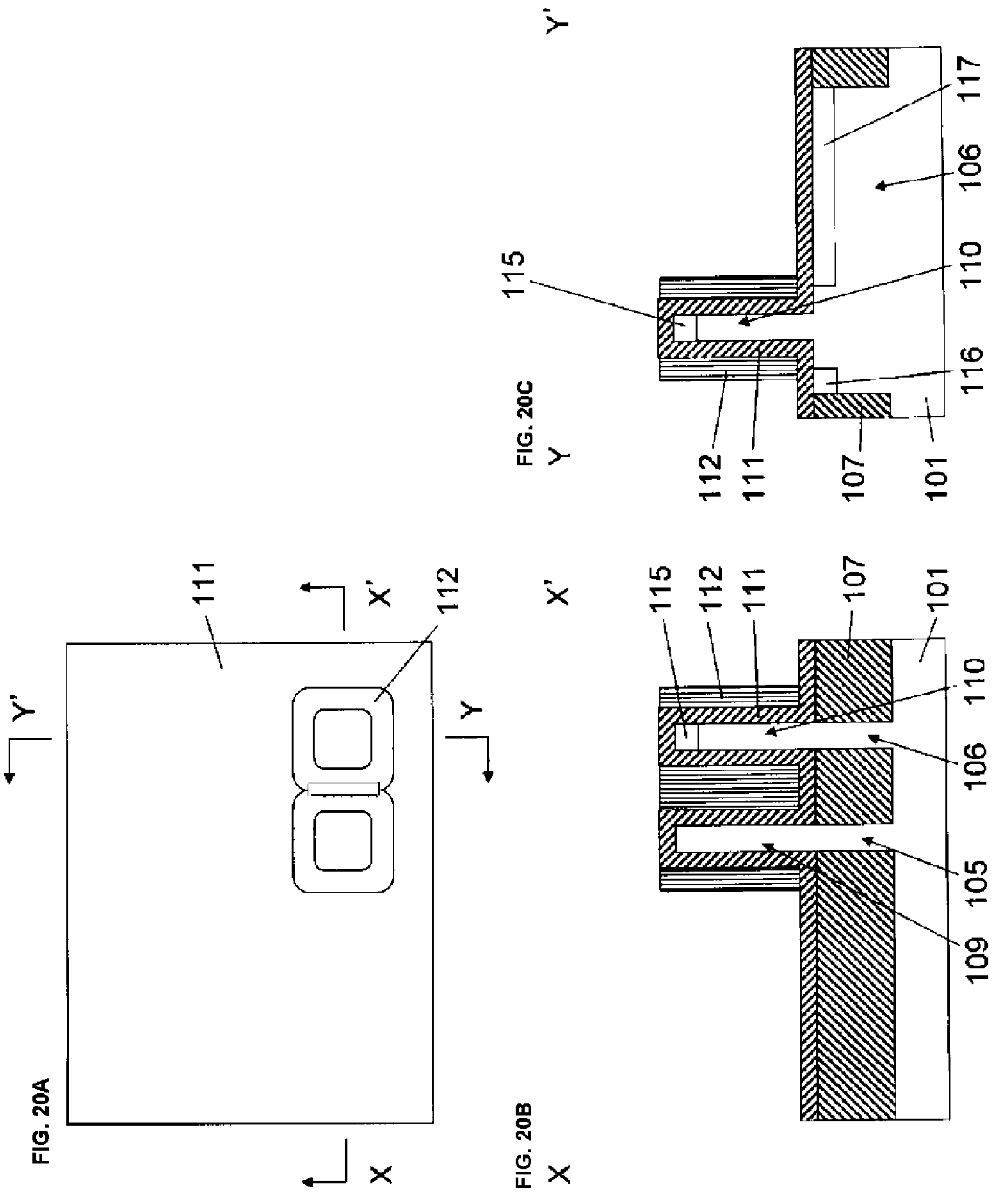


FIG. 20A
111
112
X
X'
Y
Y'
FIG. 20B
115
112
111
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110
106
105
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FIG. 20C
115
110
106
117
116
112
111
107
101

FIG. 21A

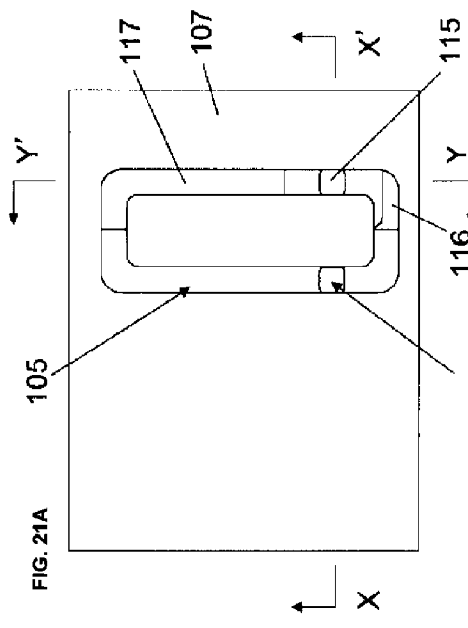


FIG. 21B

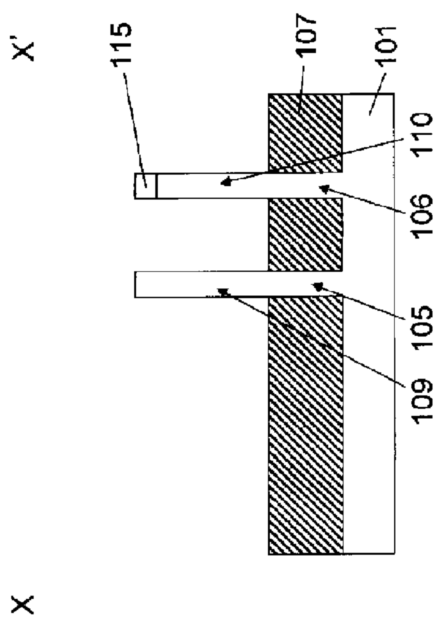
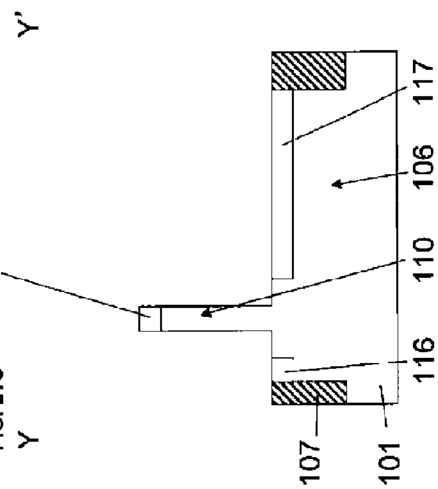


FIG. 21C



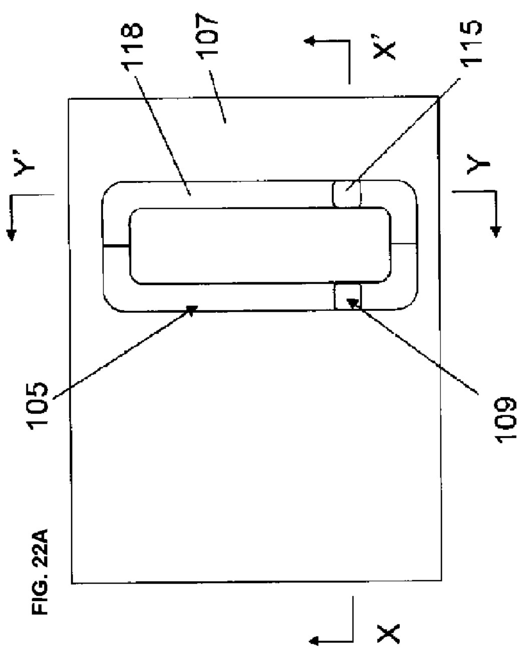


FIG. 22A

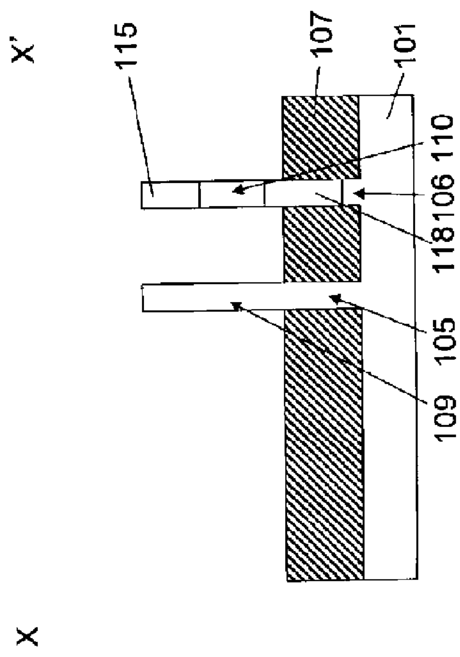


FIG. 22B

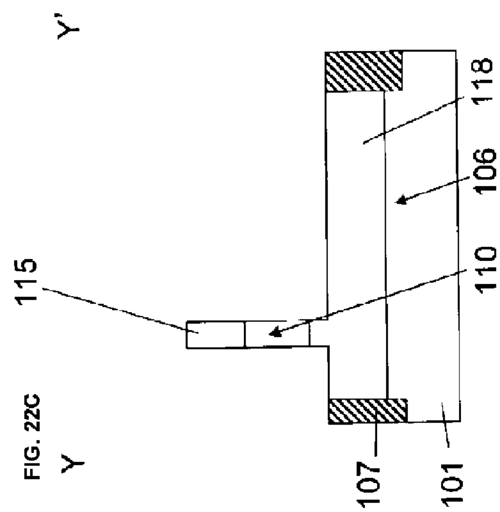


FIG. 22C

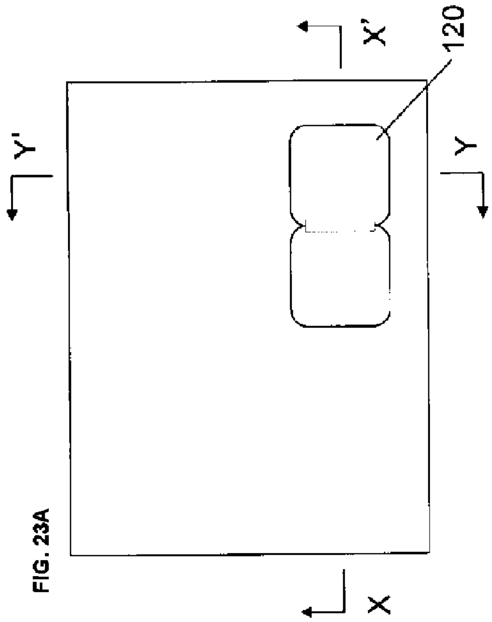


FIG. 23A

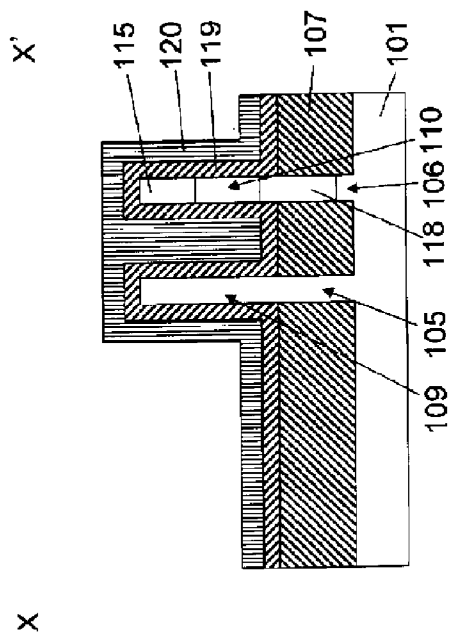


FIG. 23B

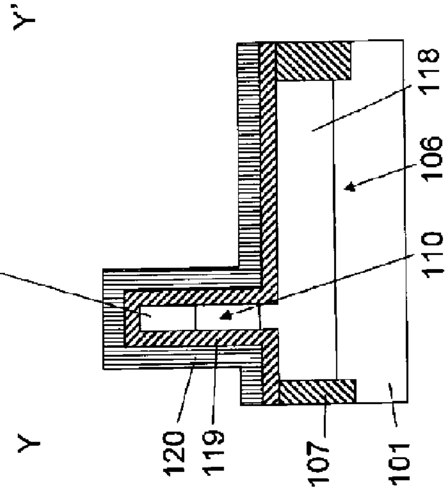


FIG. 23C

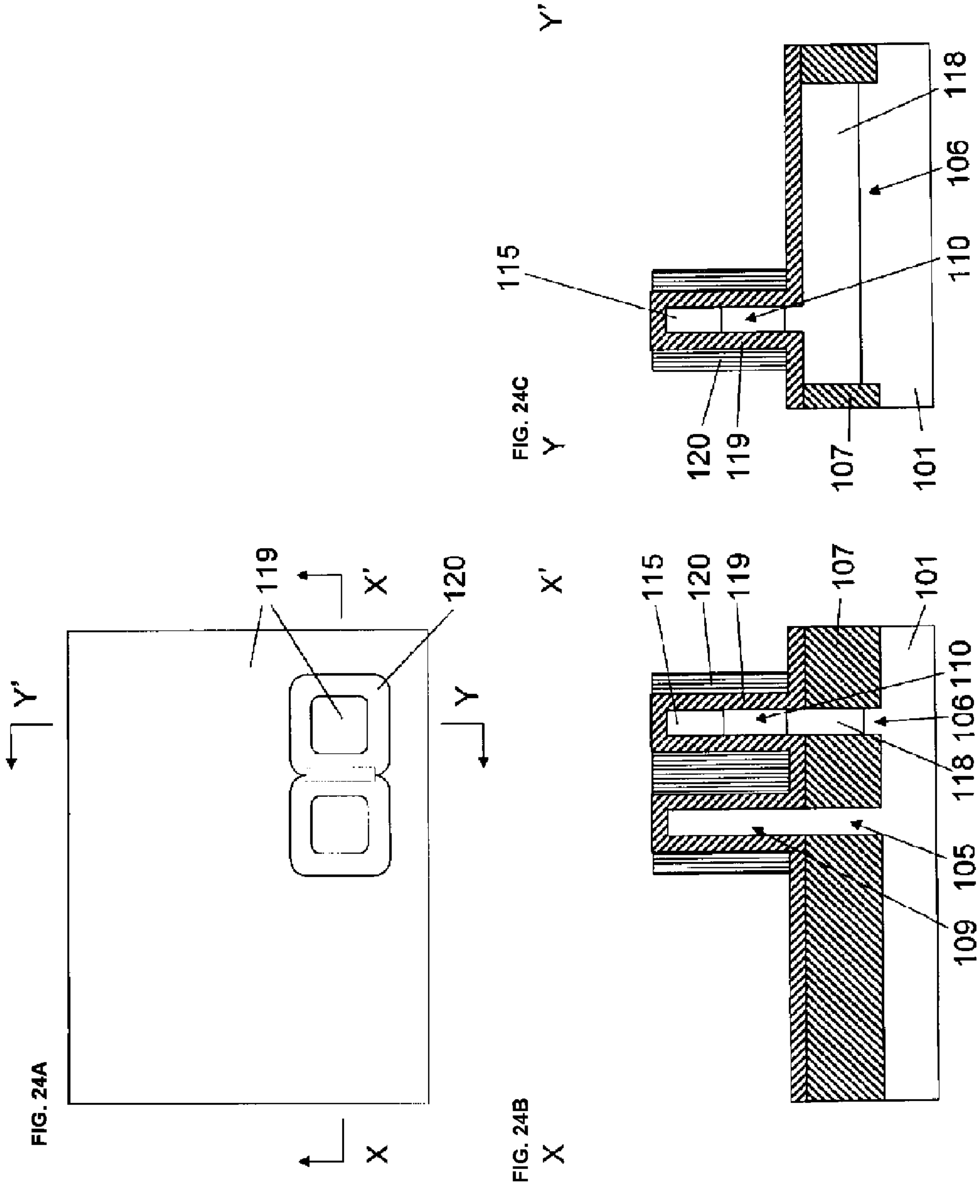


FIG. 24A

FIG. 24B

FIG. 24C

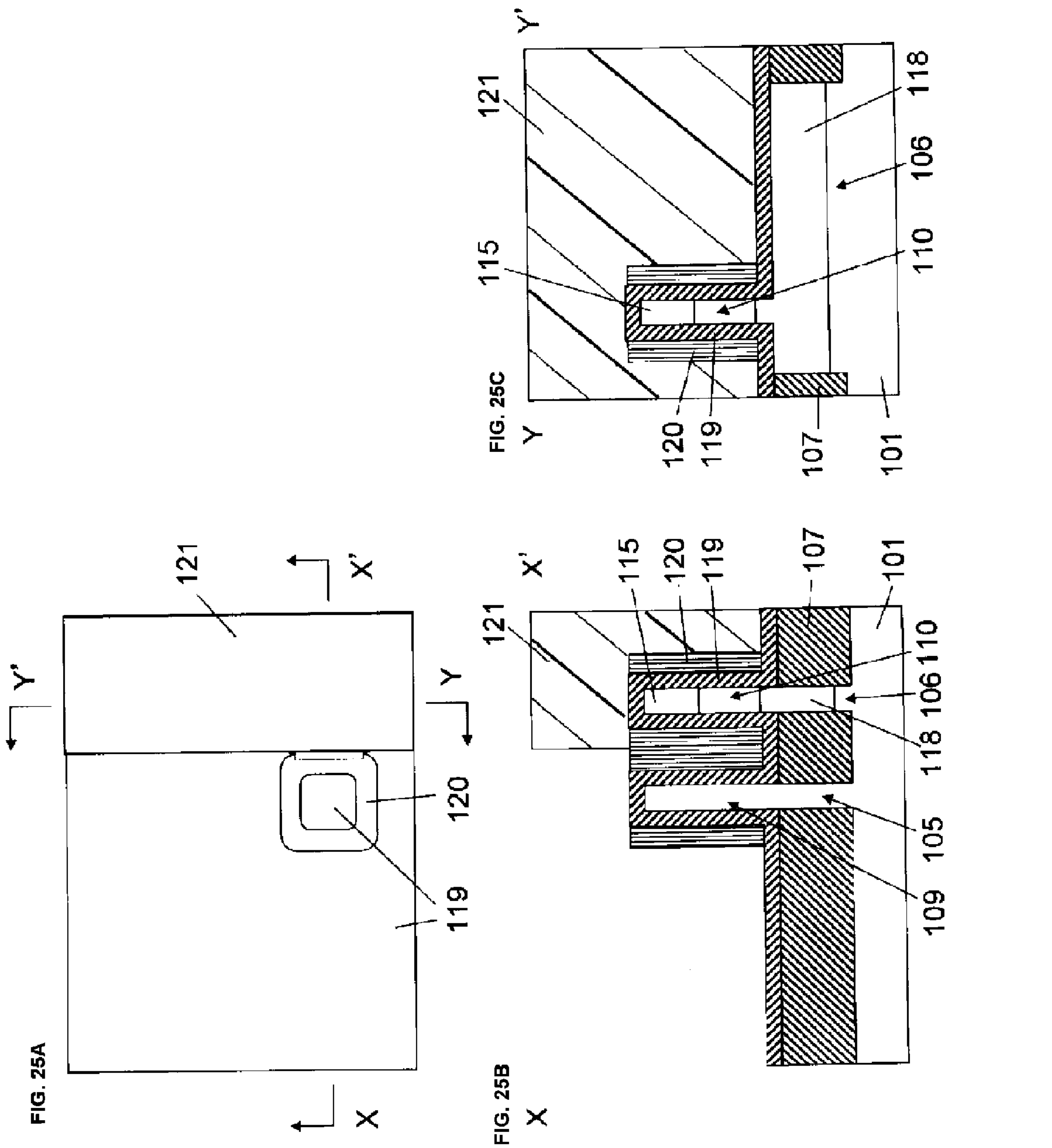


FIG. 25A
X
X'
Y
Y'
121
120
119
FIG. 25B
X
X'
121
115
120
119
107
101
110
106
118
105
109
FIG. 25C
Y
Y'
121
115
110
106
118
120
119
107
101

FIG. 26A

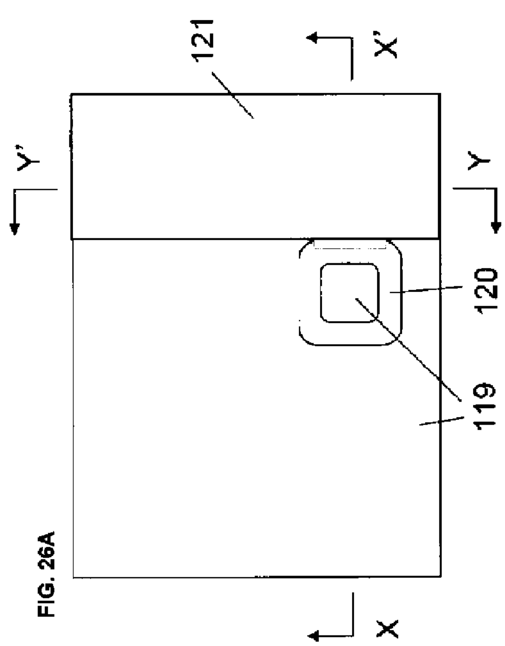


FIG. 26B

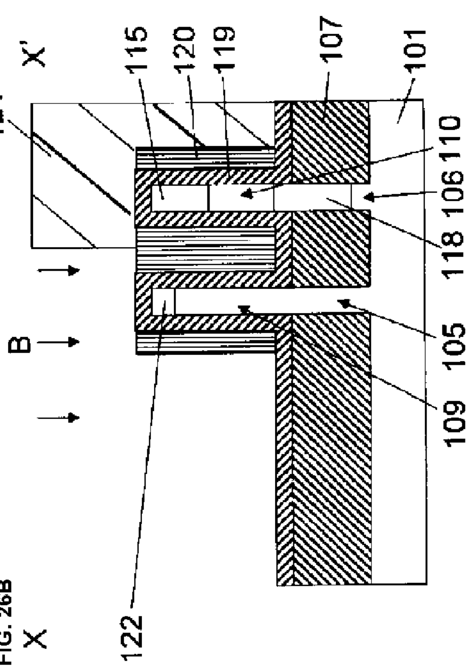
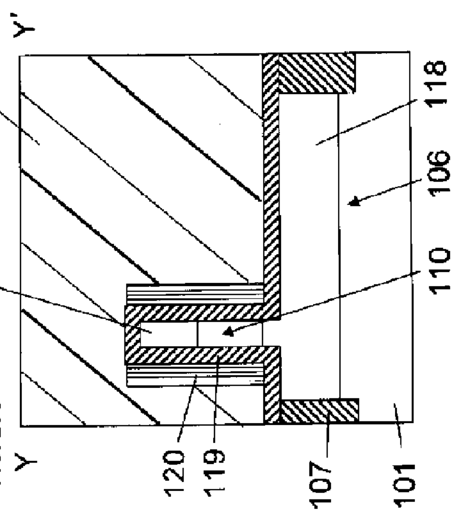


FIG. 26C



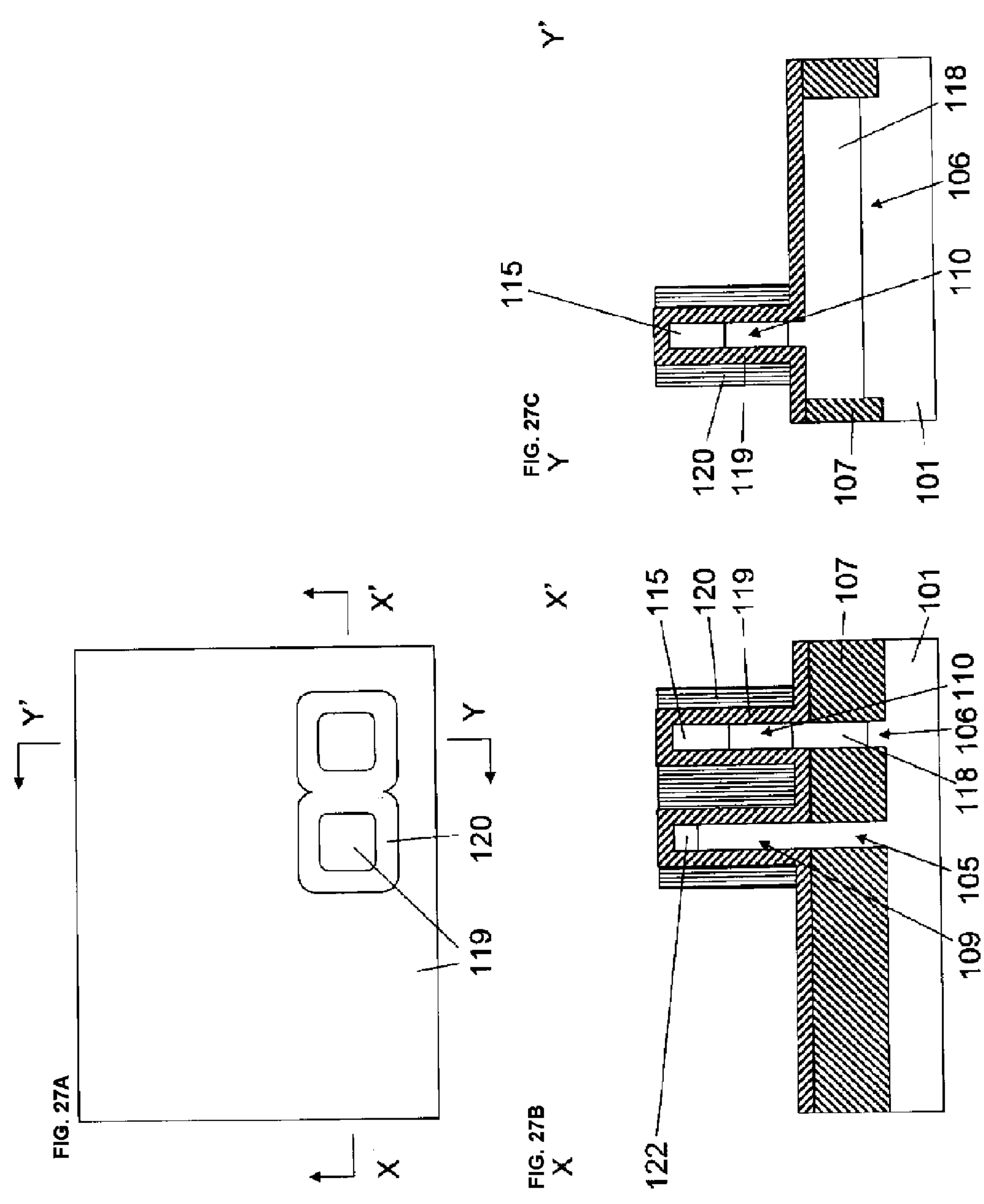


FIG. 27A

FIG. 27B

FIG. 27C

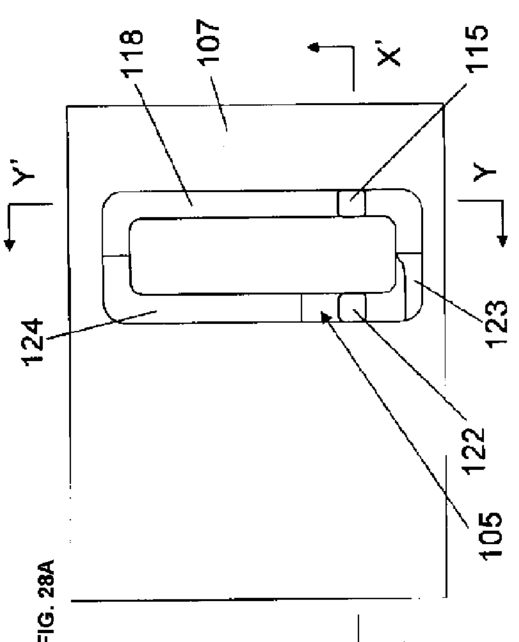


FIG. 28A

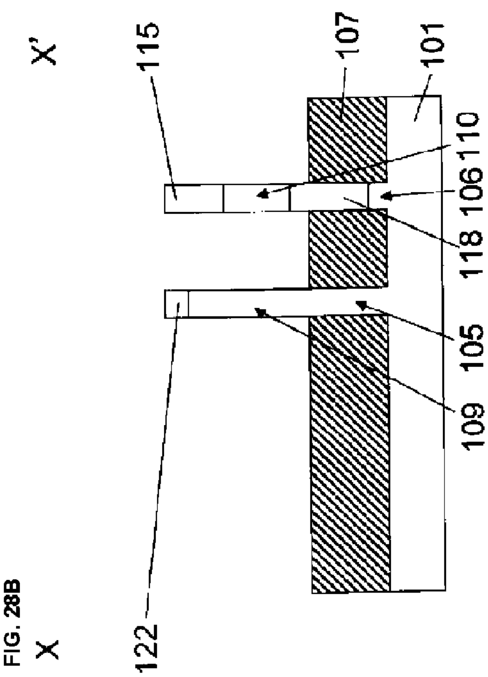


FIG. 28B

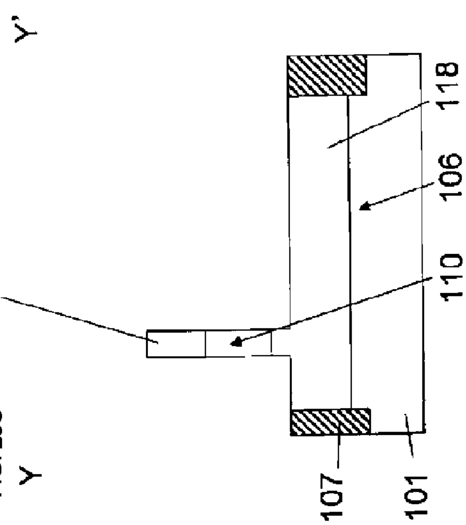


FIG. 28C

FIG. 29A

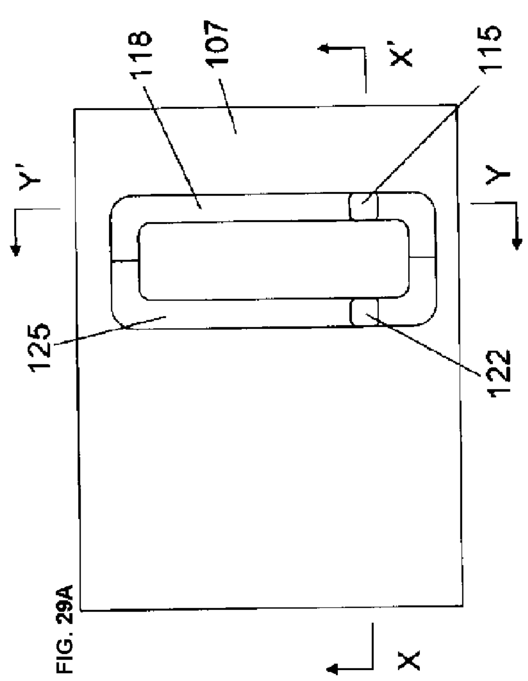


FIG. 29B

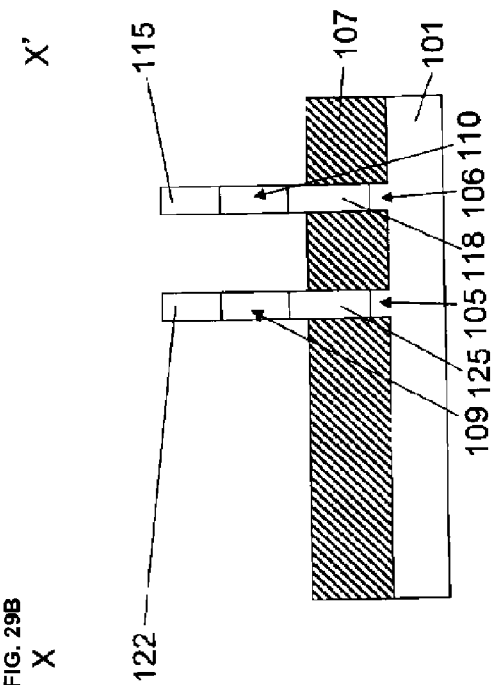
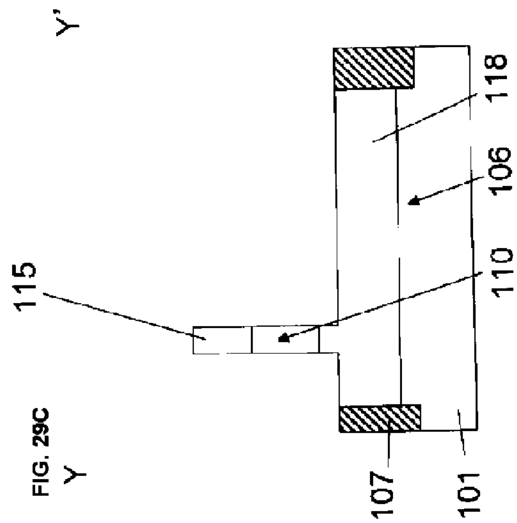


FIG. 29C



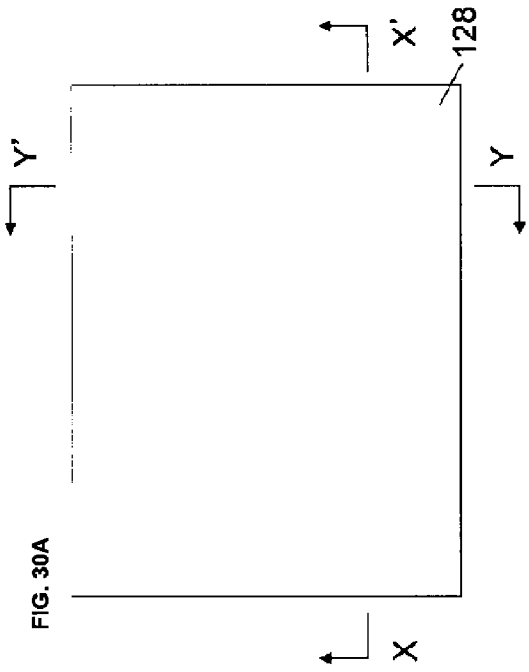


FIG. 30A

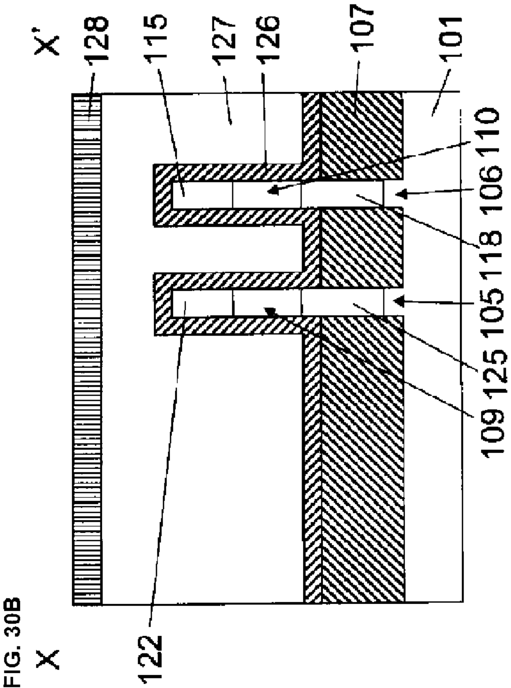


FIG. 30B

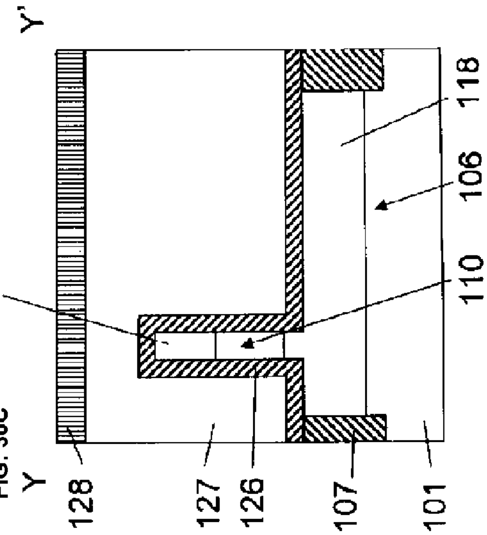


FIG. 30C

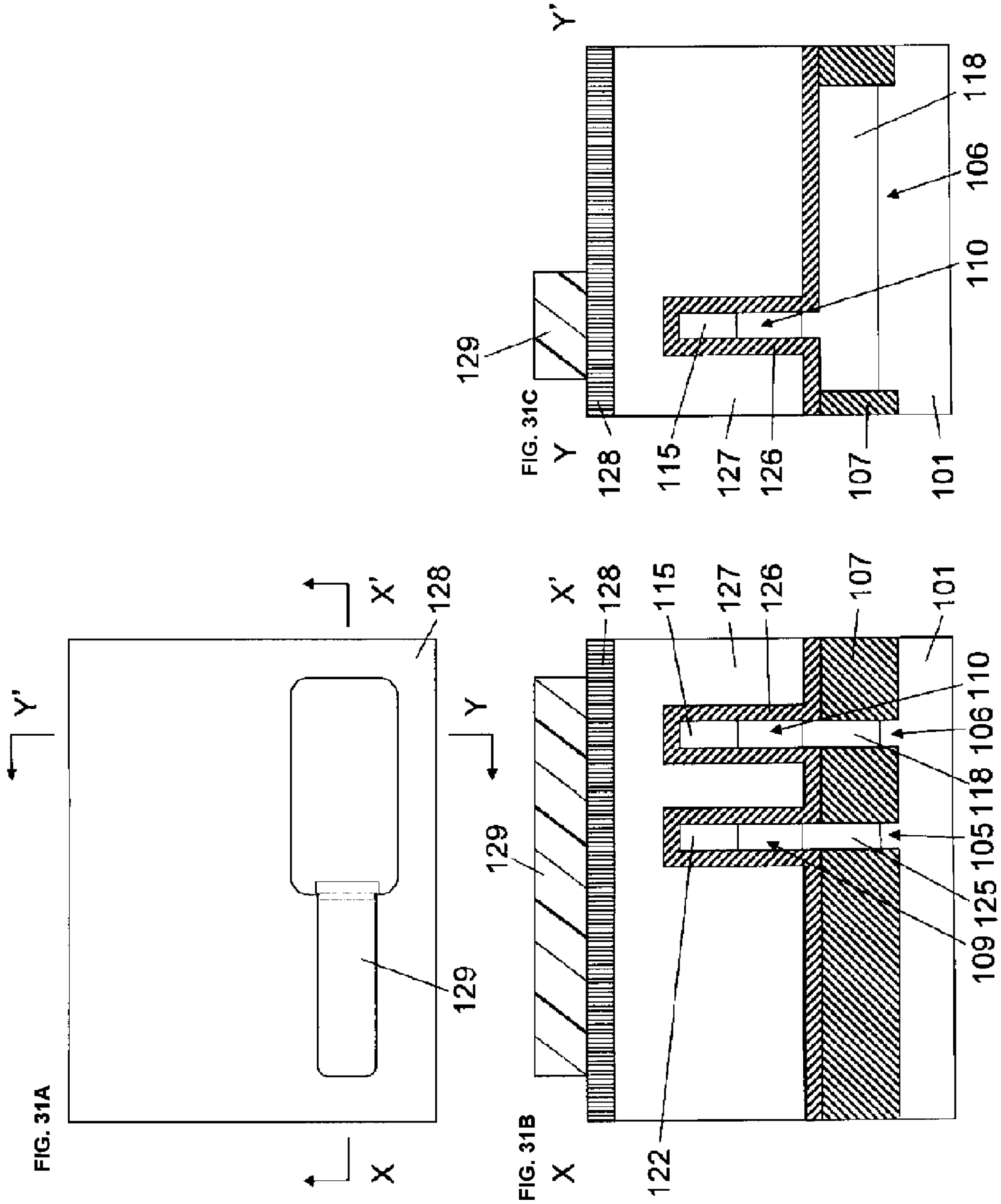


FIG. 31A
FIG. 31B
FIG. 31C
X
X'
Y
Y'
101
105
106
107
109
110
115
118
122
125
126
127
128
129

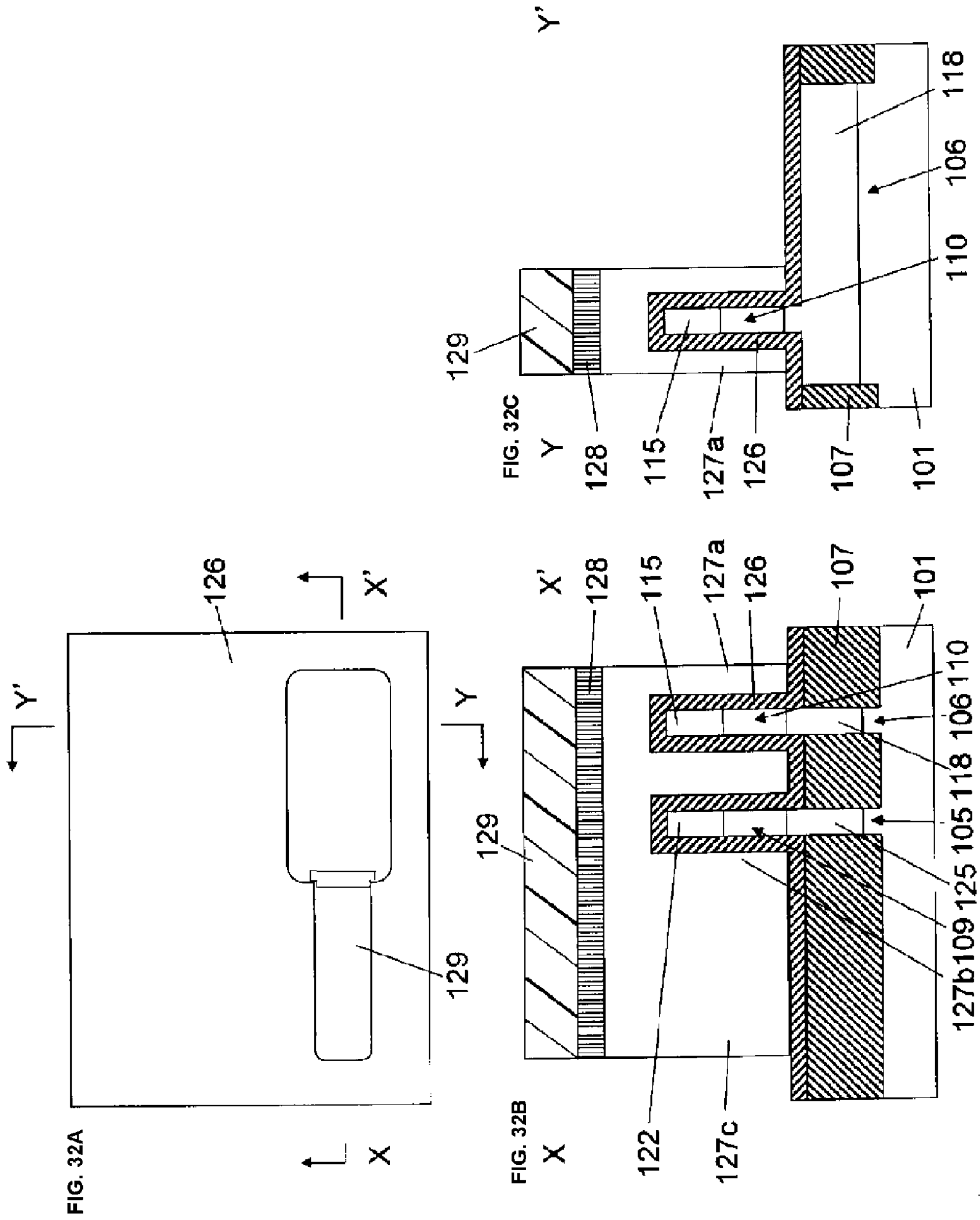


FIG. 32A
X
X'
Y
Y'
126
129
FIG. 32B
X
X'
128
115
127a
126
107
101
110
106
118
105
125
109
127b
129
122
127c
FIG. 32C
Y
Y'
129
128
115
127a
126
107
101
110
106
118

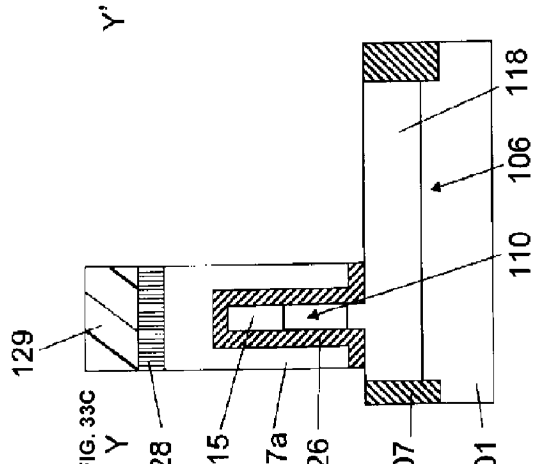


FIG. 33C

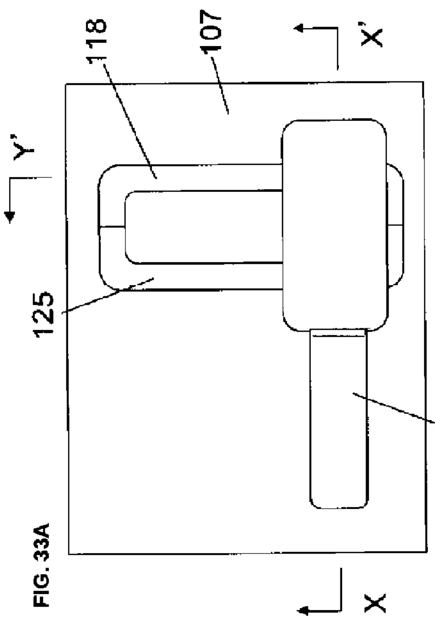


FIG. 33A

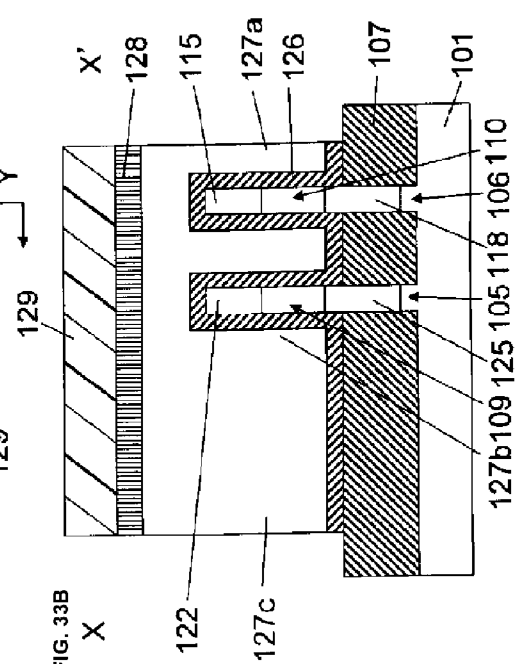


FIG. 33B

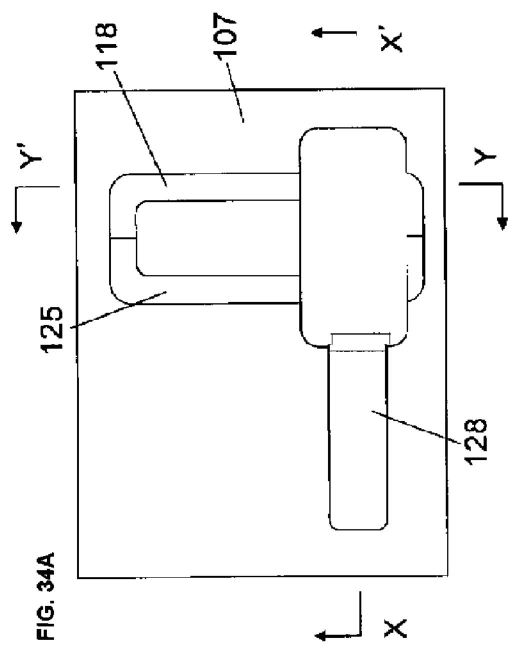


FIG. 34A

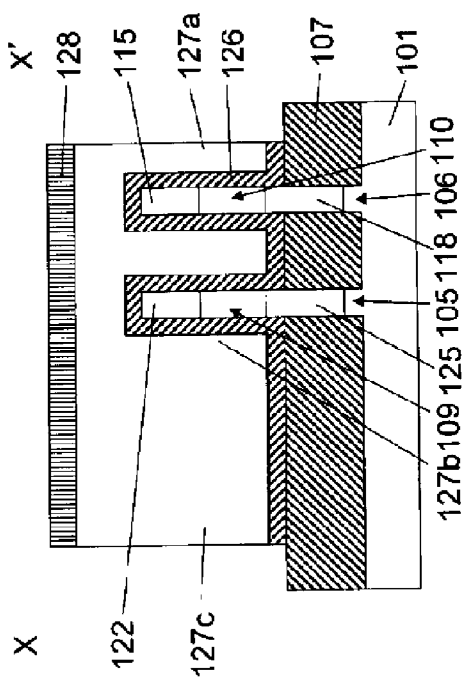


FIG. 34B

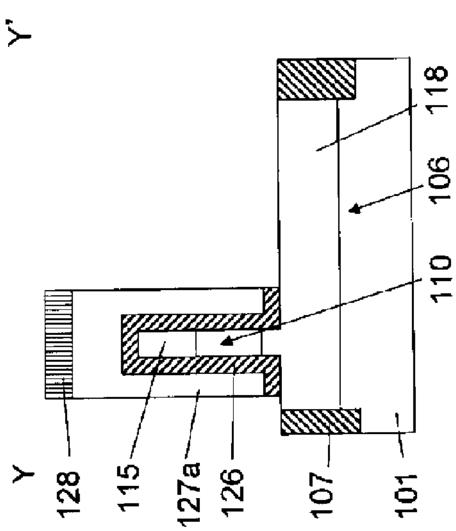


FIG. 34C

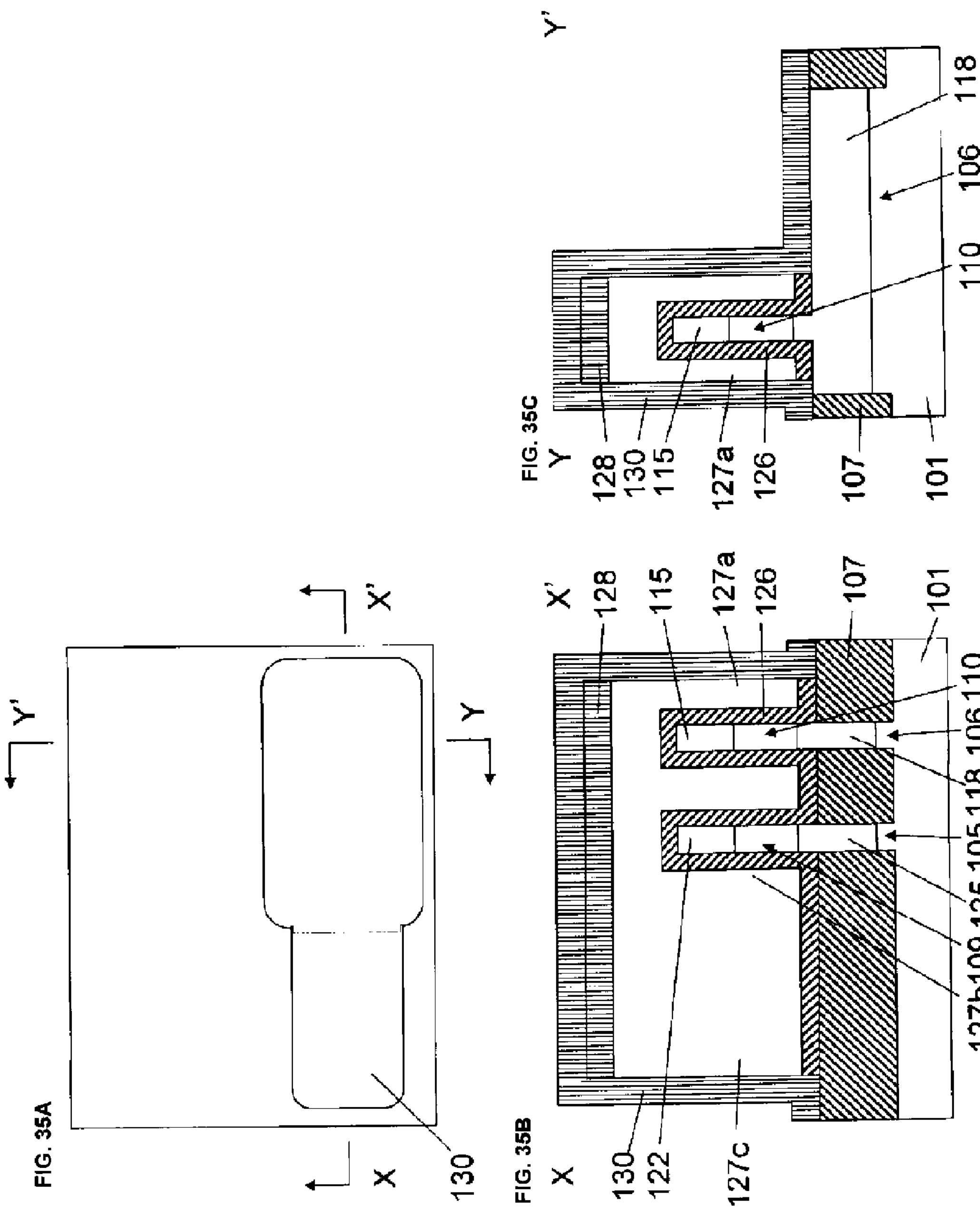


FIG. 35A
X
X'
Y
Y'
130
FIG. 35B
X
X'
130
122
127c
128
115
127a
126
107
101
110
106
118
105
125
109
127b
FIG. 35C
Y
Y'
128
130
115
127a
126
107
101
110
106
118

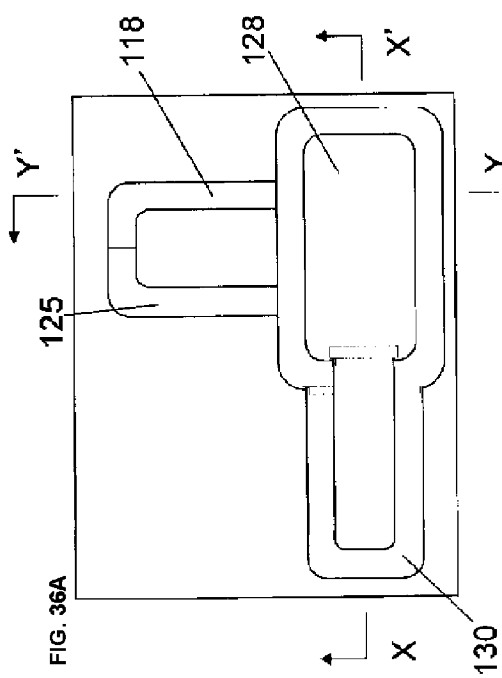


FIG. 36A

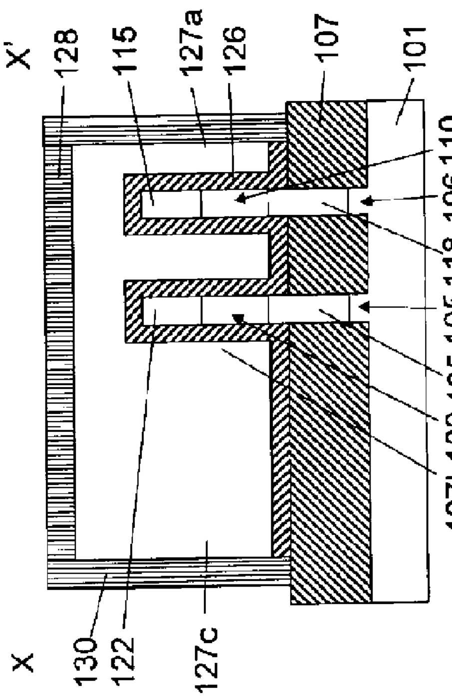


FIG. 36B

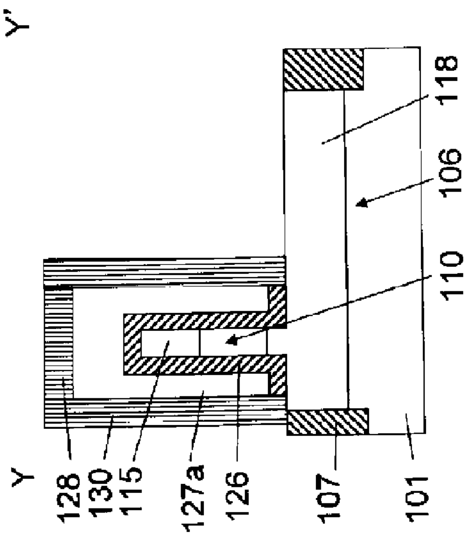


FIG. 36C

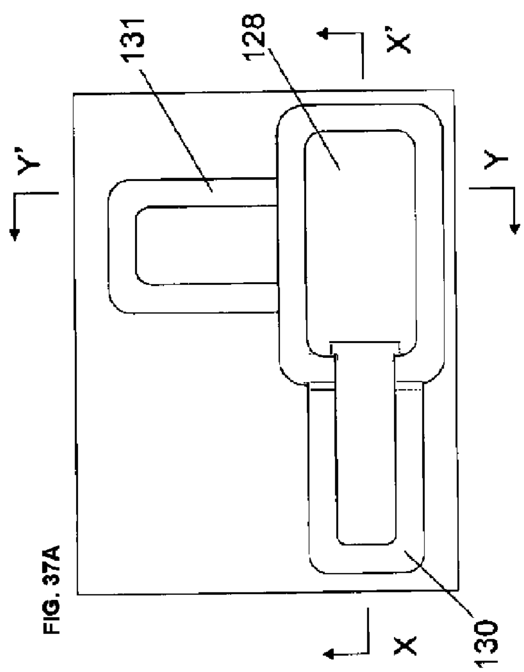


FIG. 37A

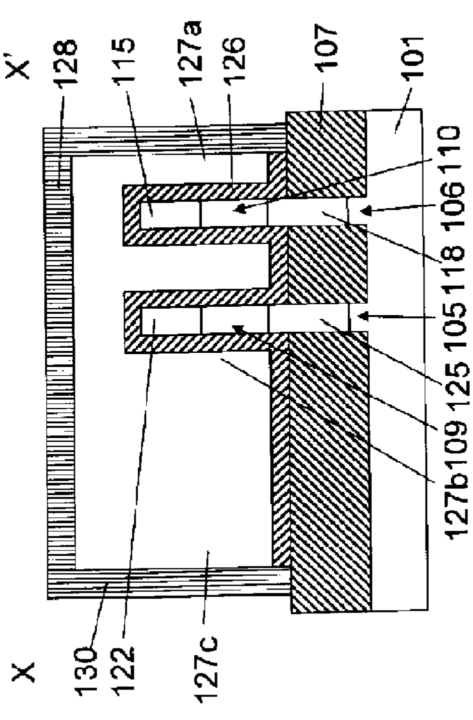


FIG. 37B

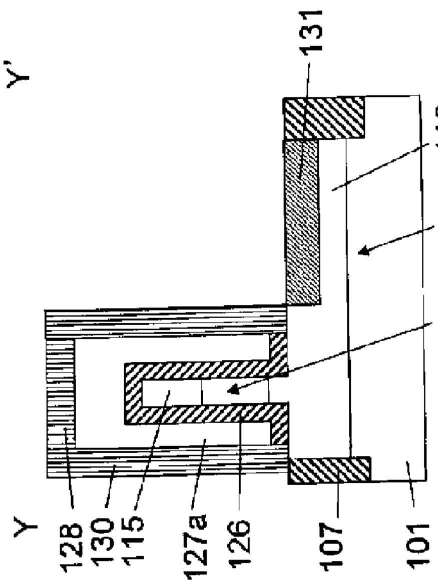


FIG. 37C

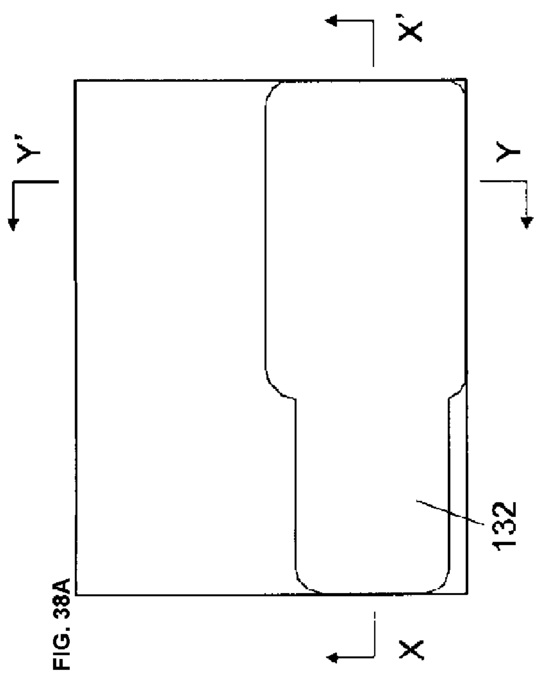


FIG. 38A

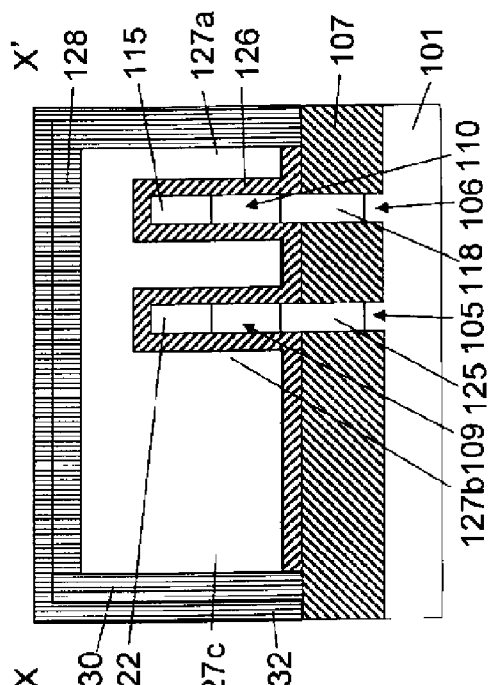


FIG. 38B

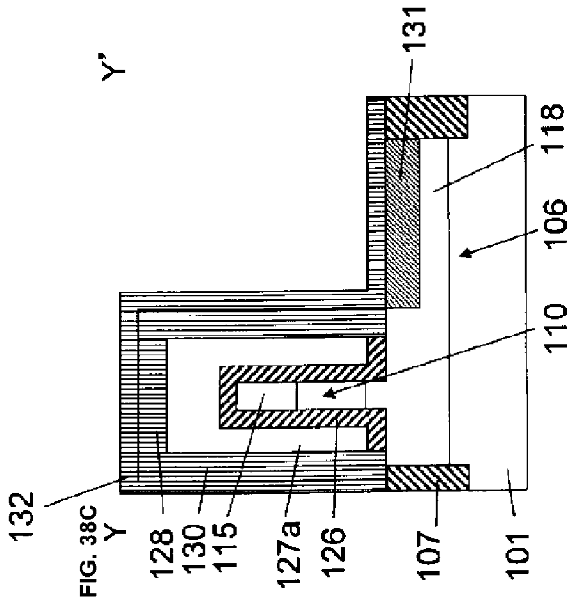


FIG. 38C

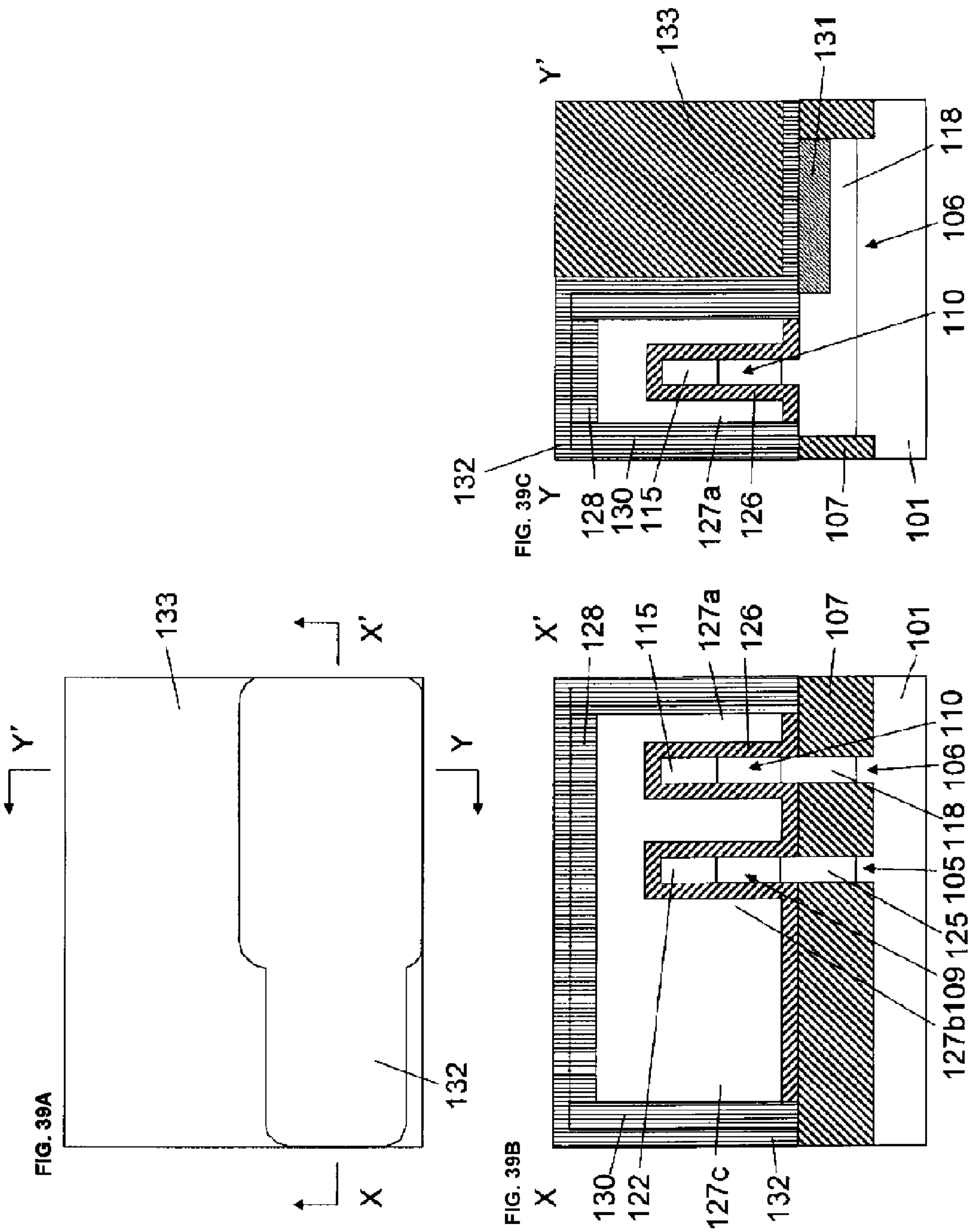


FIG. 39A
Y'
Y
X
X'
133
132
FIG. 39B
X
X'
130
122
127c
132
128
115
127a
126
107
101
110
106
118
105
125
109
127b
FIG. 39C
Y
Y'
132
128
130
115
127a
126
107
101
110
106
118
131
133

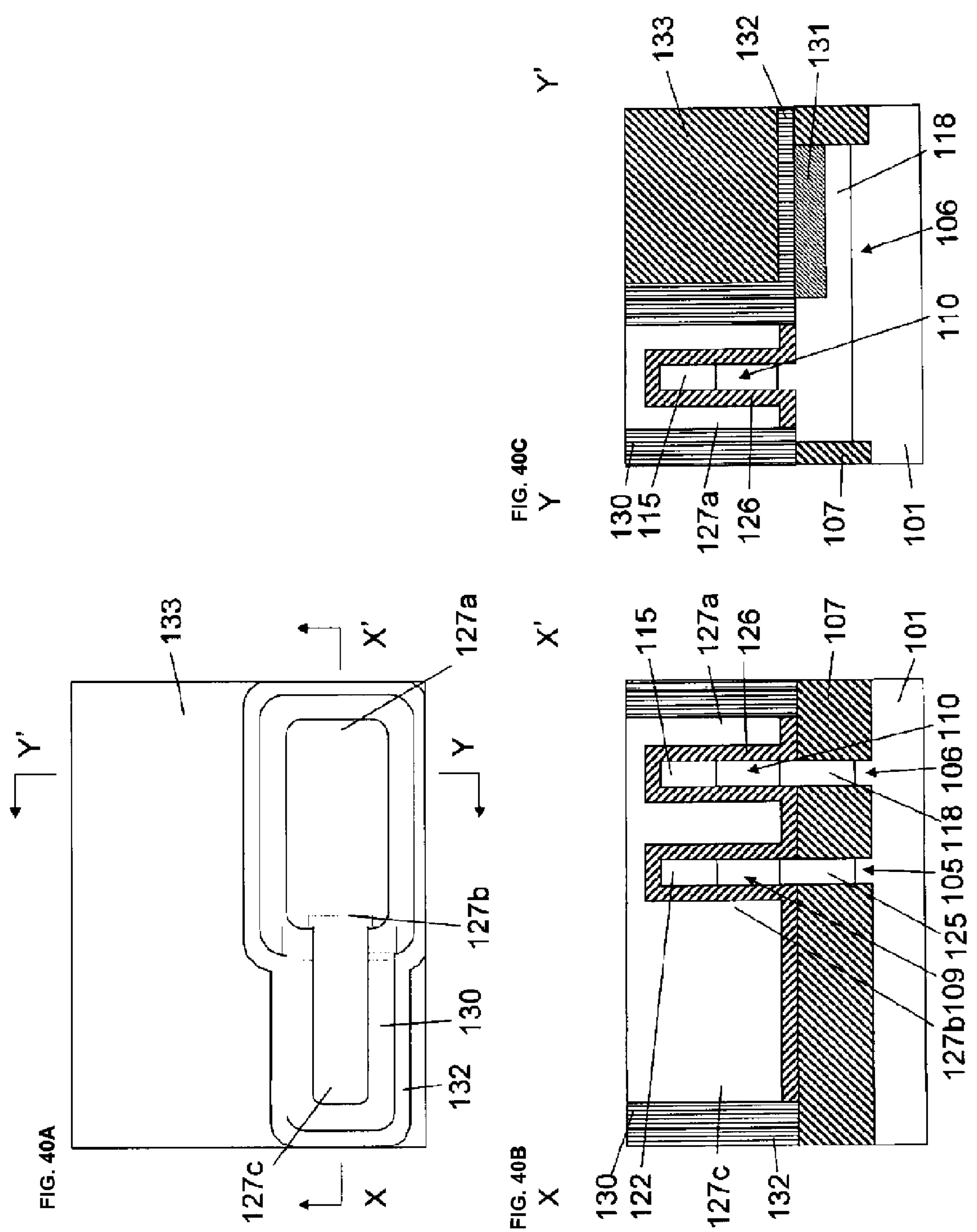


FIG. 40A

FIG. 40B

FIG. 40C

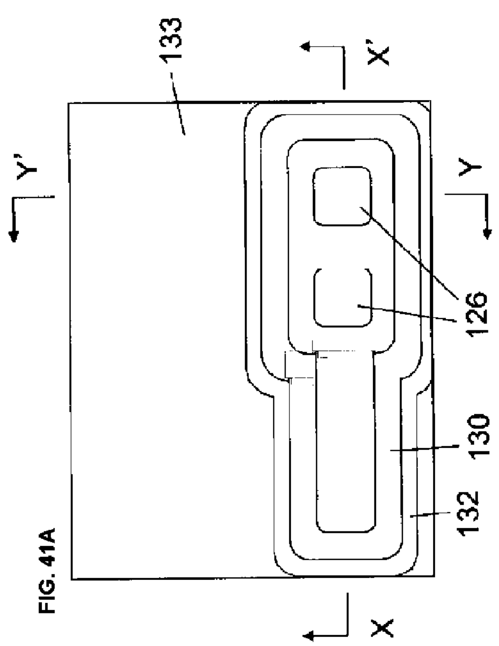


FIG. 41A

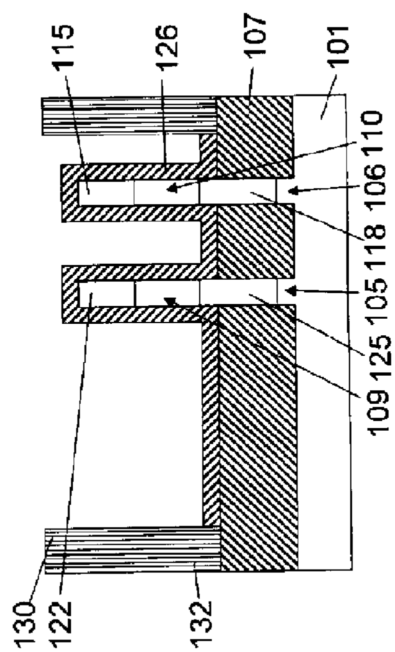


FIG. 41B

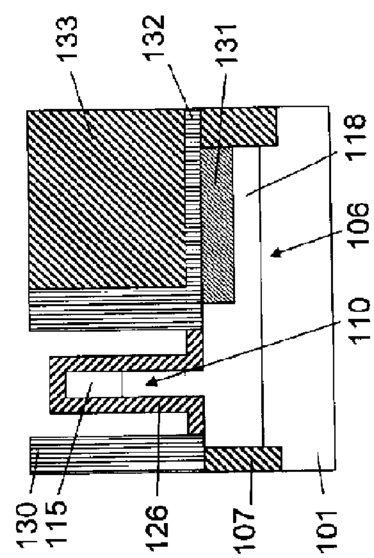


FIG. 41C

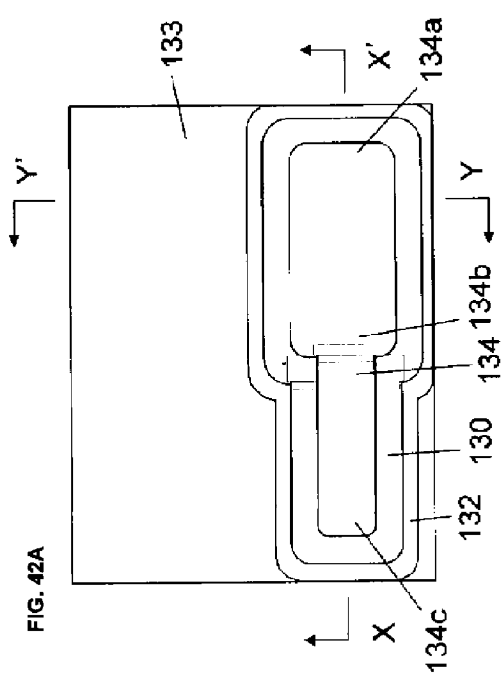


FIG. 42A

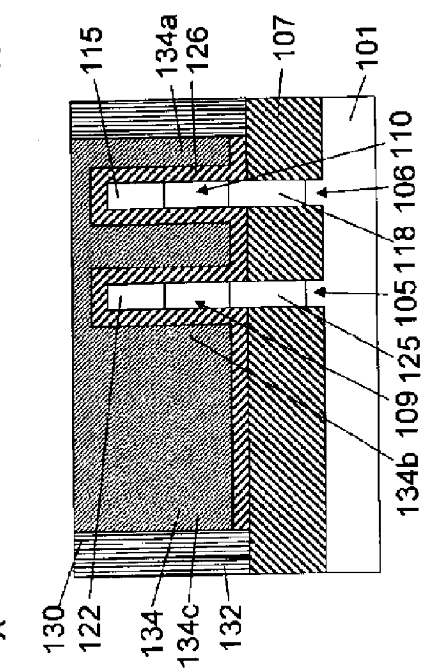


FIG. 42B

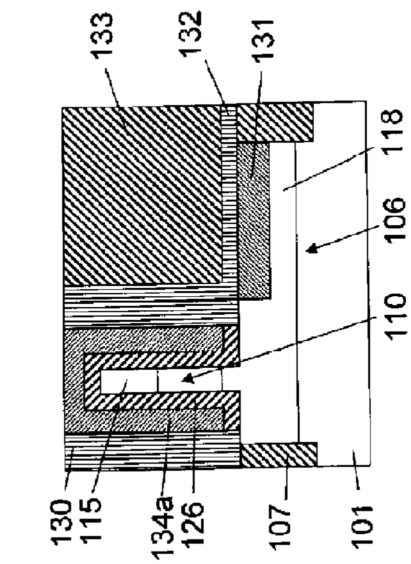


FIG. 42C

FIG. 43A

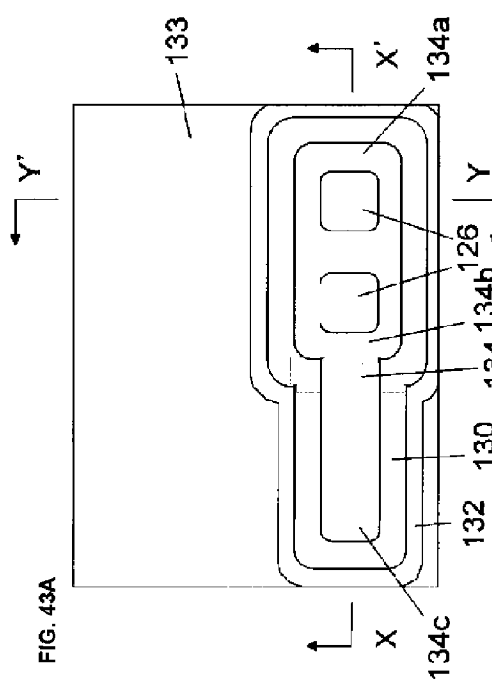


FIG. 43B

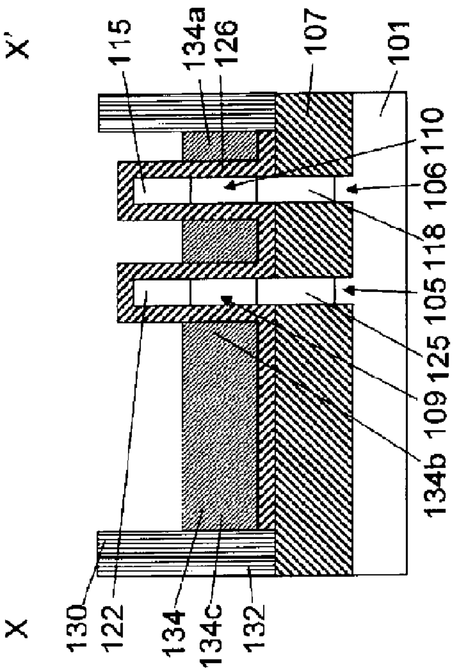


FIG. 43C

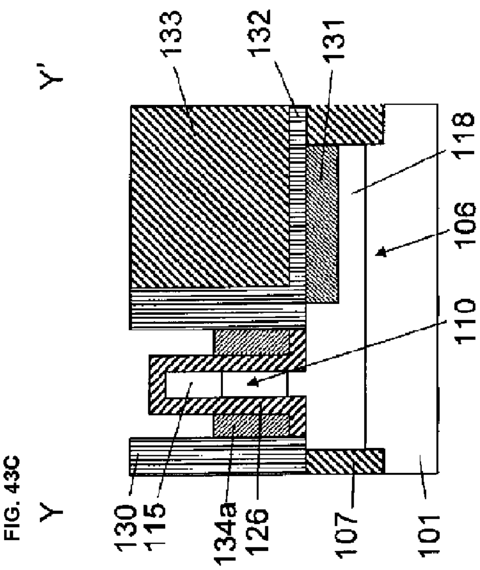


FIG. 44A

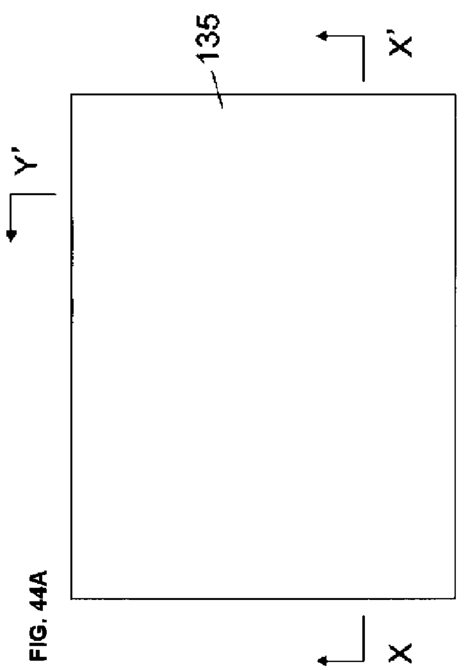


FIG. 44B

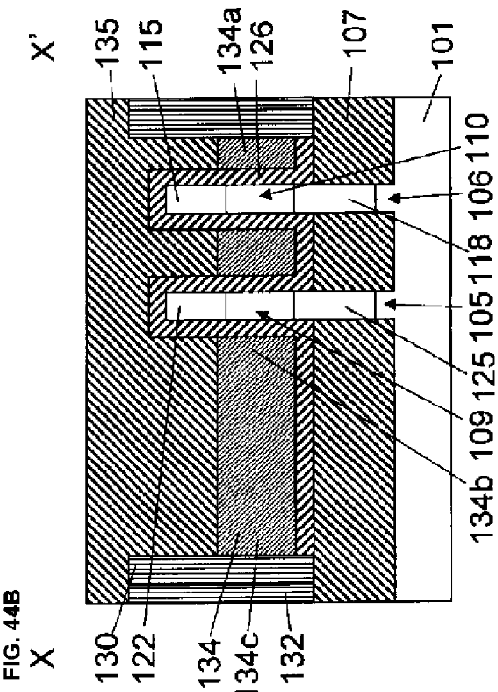
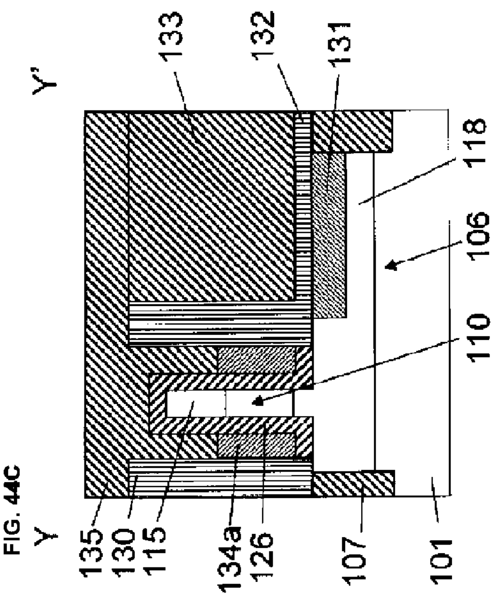


FIG. 44C



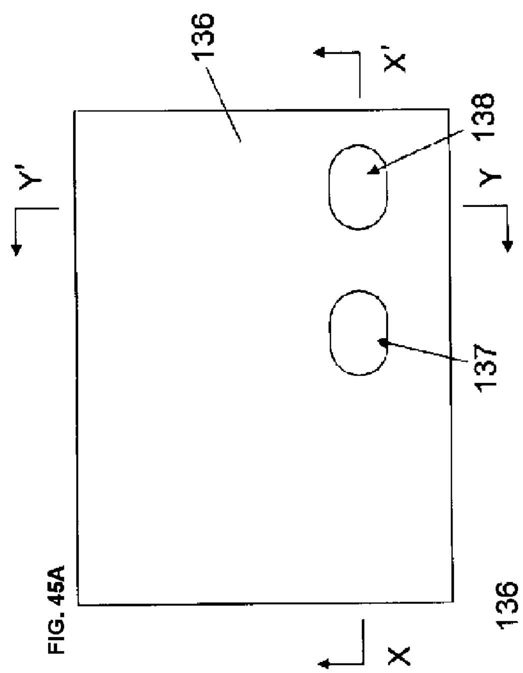


FIG. 45A

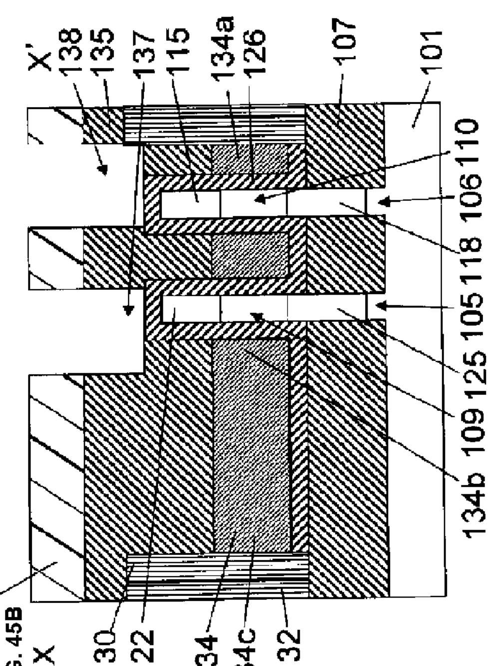


FIG. 45B

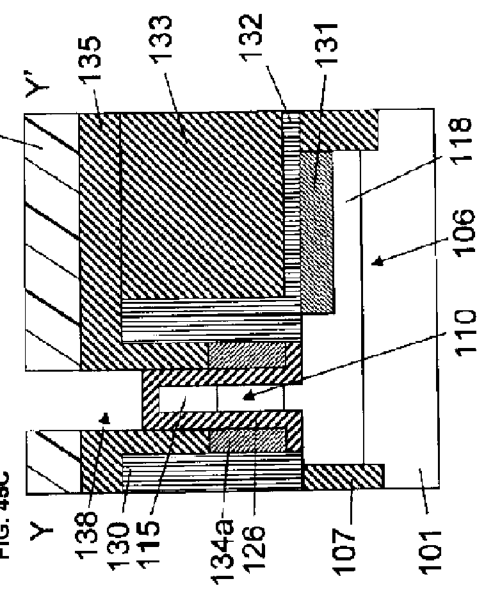


FIG. 45C

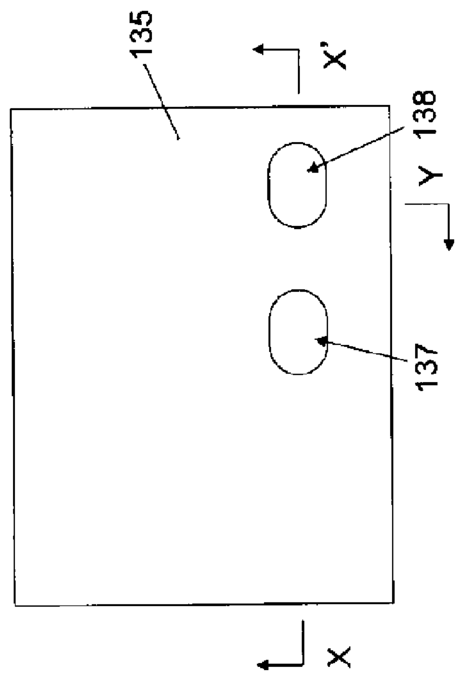


FIG. 46A

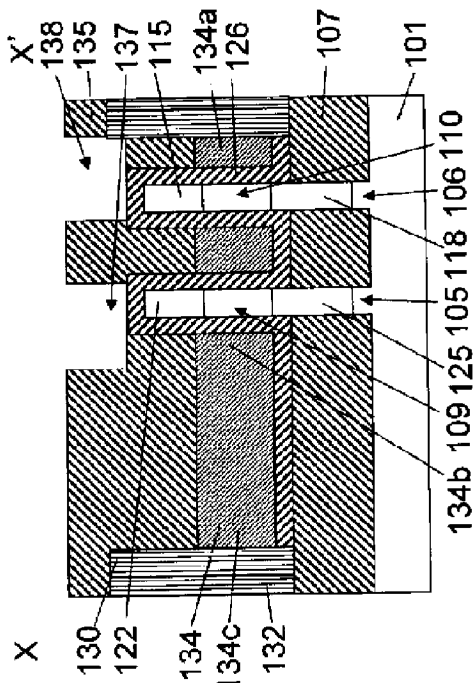


FIG. 46B

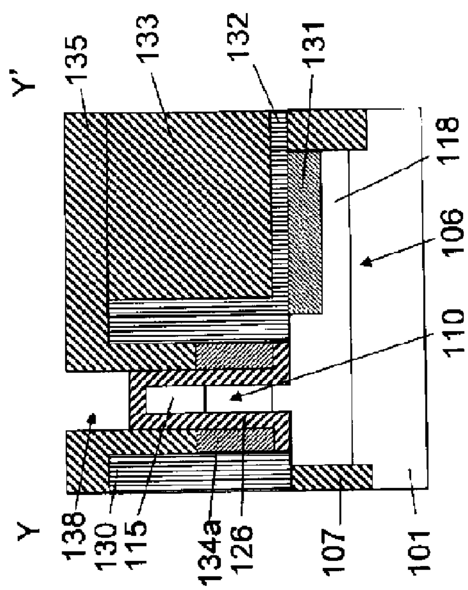


FIG. 46C

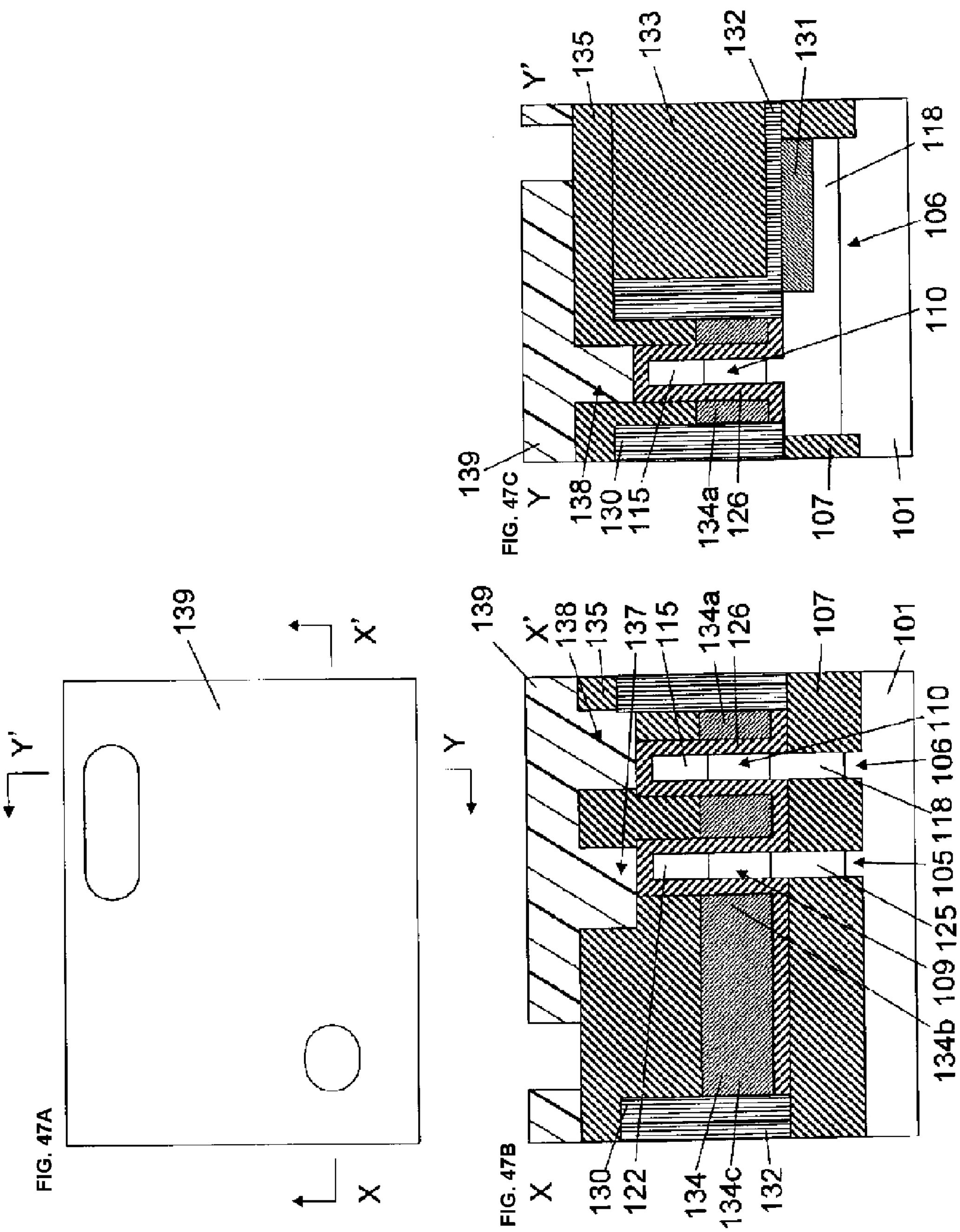


FIG. 47A

FIG. 47B

FIG. 47C

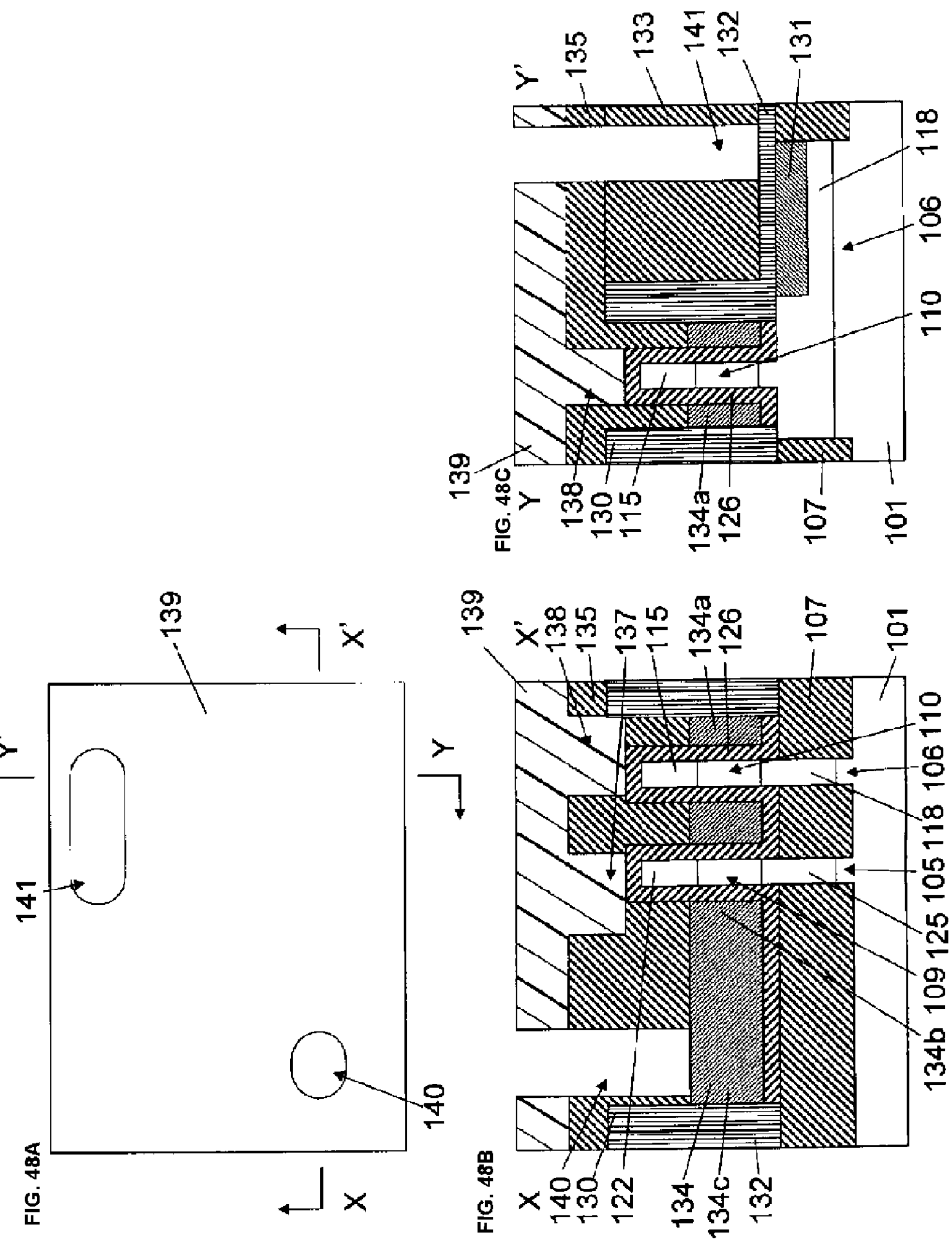


FIG. 48A
FIG. 48B
FIG. 48C
X
X'
Y
Y'
139
140
141
101
105
106
107
109
110
115
118
122
125
126
130
131
132
133
134
134a
134b
134c
135
137
138

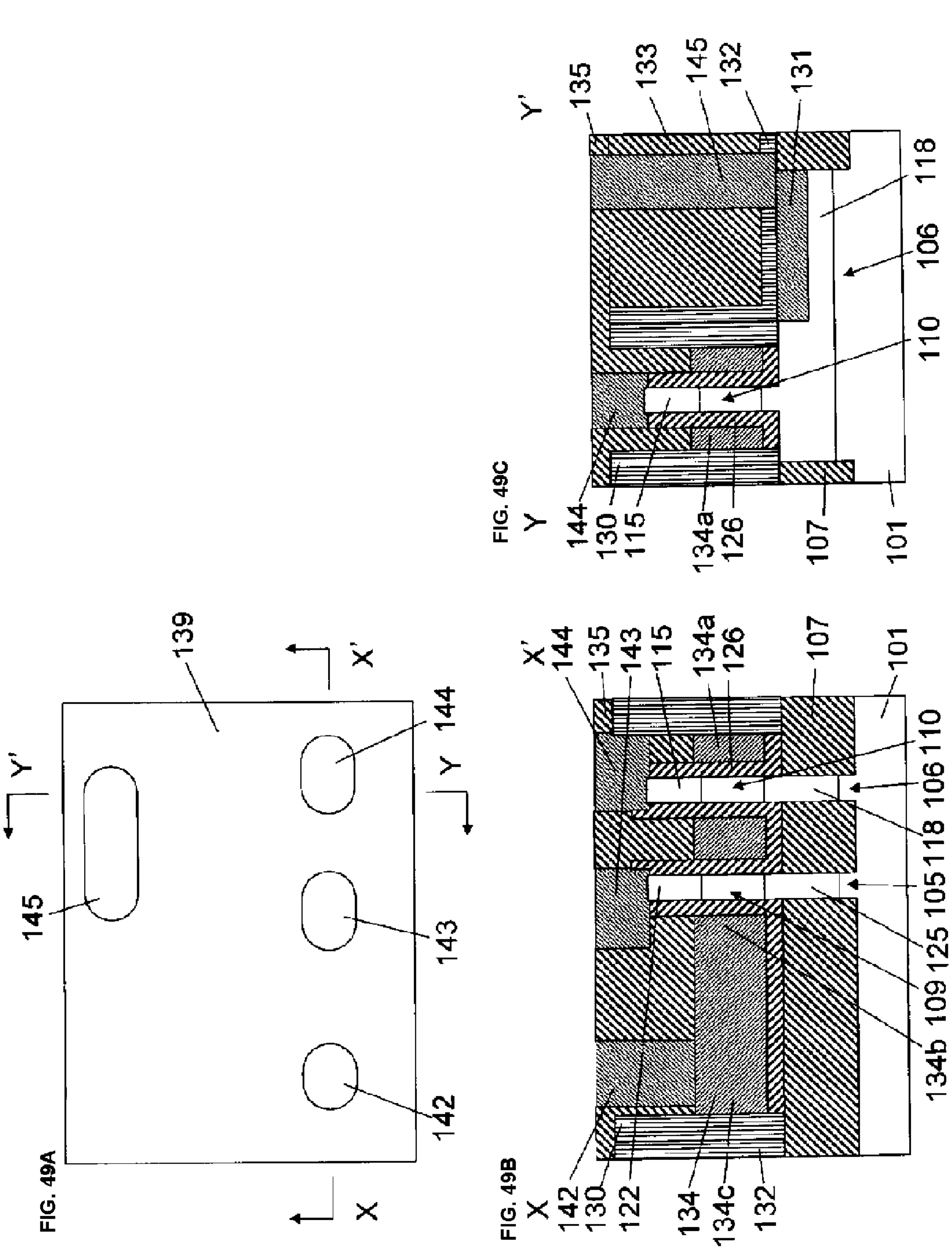


FIG. 49A
FIG. 49B
FIG. 49C
X
X'
Y
Y'
139
142
143
144
145
130
122
134
134c
132
135
115
134a
126
107
101
110
106
118
105
125
109
134b
133
131

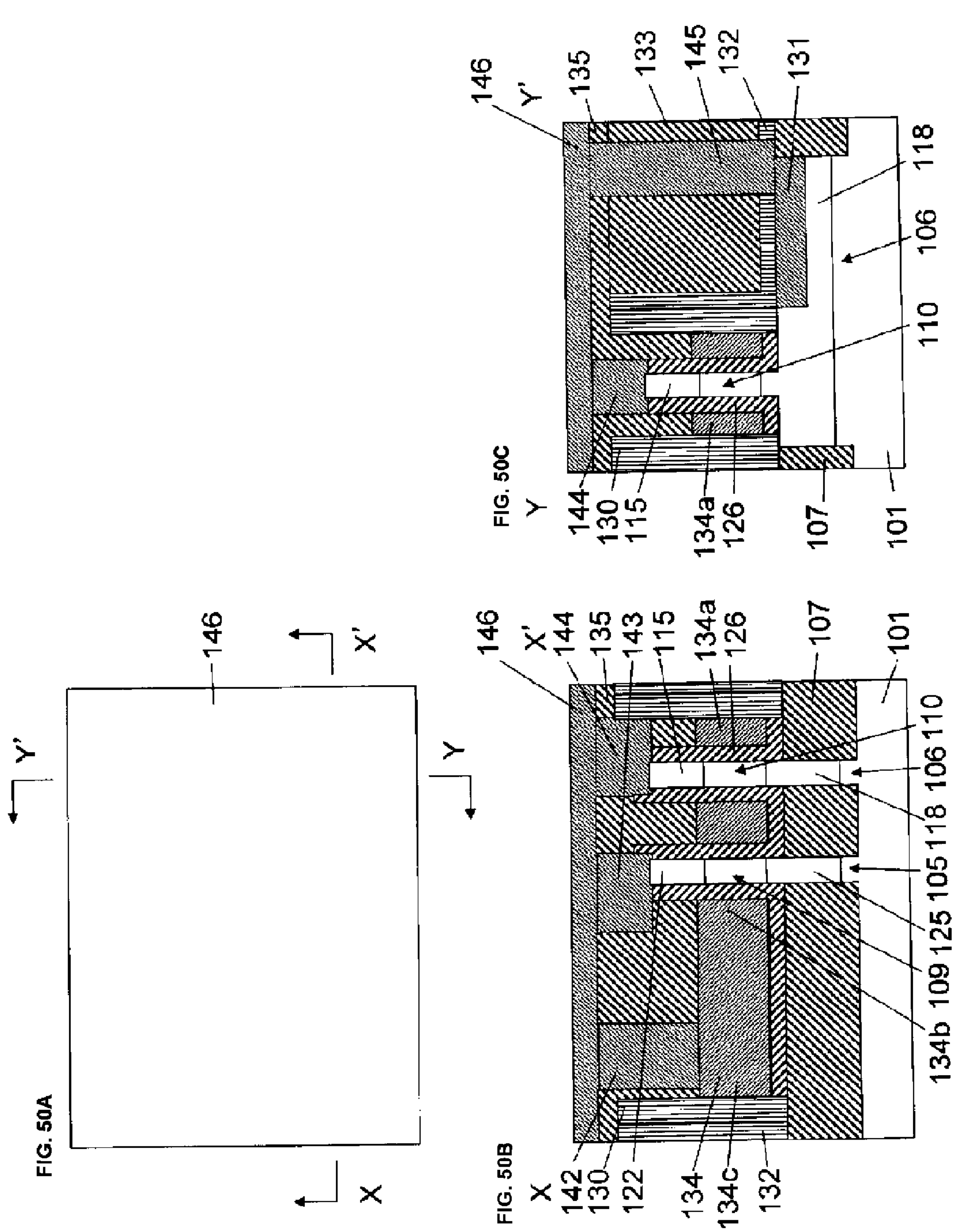


FIG. 50A
FIG. 50B
FIG. 50C

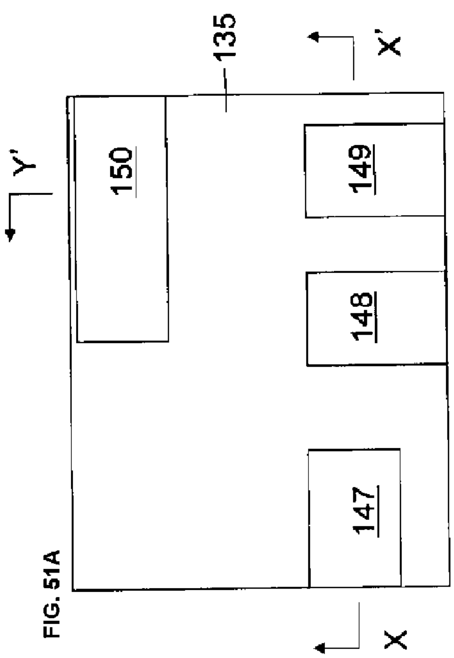


FIG. 51A

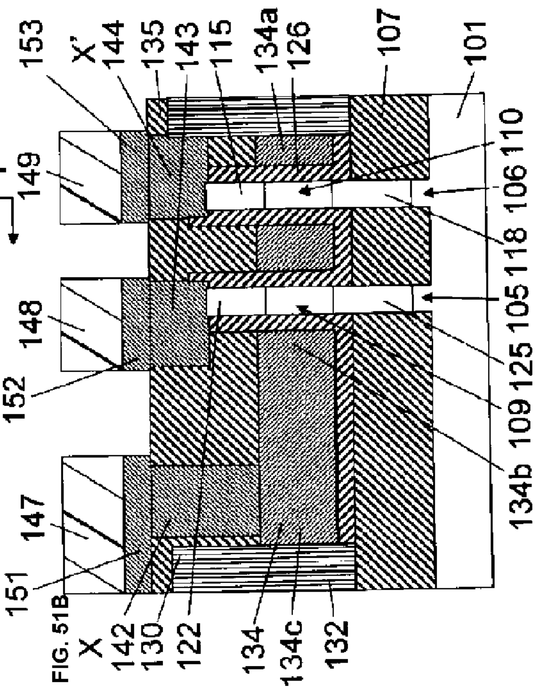


FIG. 51B

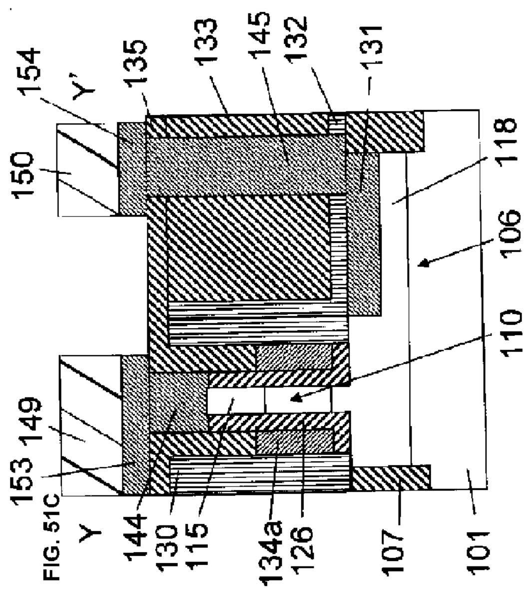


FIG. 51C

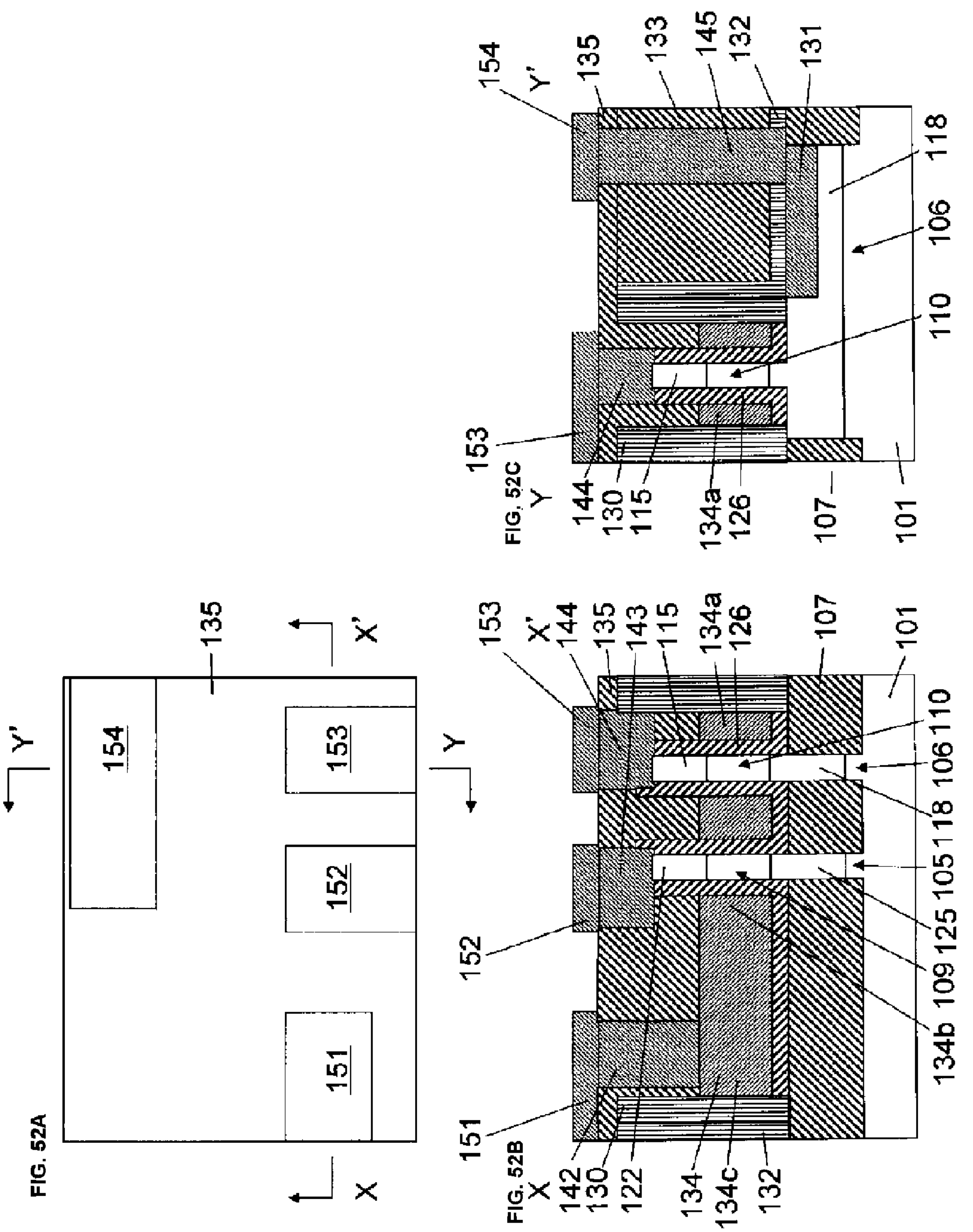


FIG. 52A

FIG. 52B

FIG. 52C

METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE

RELATED APPLICATIONS

This application is a continuation application of U.S. patent application Ser. No. 14/537,322, filed Nov. 10, 2014, now U.S. Pat. No. 9,245,889, which is a continuation application of U.S. patent application Ser. No. 14/006,095, filed Oct. 29, 2013, now U.S. Pat. No. 8,916,478, which is a Continuation-In-Part (CIP) application of U.S. patent application Ser. No. 13/693,524, filed Dec. 4, 2012, now U.S. Pat. No. 8,772,175, which pursuant to 35 U.S.C. §119(e), claims the benefit of the filing date of Provisional U.S. Patent Application Ser. No. 61/577,189 filed Dec. 19, 2011. The entire contents of which are hereby incorporated by reference.

BACKGROUND

1. Technical Field

The present invention relates to a method for manufacturing a semiconductor device and to a semiconductor device.

2. Description of the Related Art

Semiconductor integrated circuits, particularly integrated circuits using MOS transistors, are increasing in integration. With increases in integration, MOS transistors used in the integrated circuits are increasingly made finer up to a nano region. Finer MOS transistors have the problem of difficulty in suppressing leak currents and difficulty in decreasing the areas occupied by circuits because of the demand for securing necessary amounts of currents. In order to resolve the problem, there have been proposed surrounding gate transistors (SGT) having a structure in which a source, a gate, and a drain are disposed in a direction vertical to a substrate, and the gate surrounds a pillar-shaped semiconductor layer (for example, Japanese Unexamined Patent Application Publication Nos. 2-71556, 2-188966, and 3-145761).

By using a metal for a gate electrode instead of using polysilicon, depletion can be suppressed, and the resistance of the gate electrode can be decreased. However, a manufacturing process after a metal gate is formed must be one in which metal contamination by the metal gate is always taken into consideration.

In addition, in order to satisfy both a metal gate process and a high-temperature process for usual MOS transistors, a metal gate last process is used for actual products, in which a metal gate is formed after a high-temperature process (IEDM 2007 K. Mistry, et. al., pp. 247-250). The gate is formed using polysilicon, and then an interlayer insulating film is deposited. Then, the polysilicon gate is exposed by chemical mechanical polishing and etched, followed by deposition of a metal. Therefore, in order to satisfy both the metal gate process and the high-temperature process, the metal gate last process must be used for SGT, in which a metal gate is formed after the high-temperature process. Since, in the SGT, the top position of the pillar-shaped silicon layer is higher than the gate, some consideration is required for using the metal gate last process.

In addition, usual MOS transistors use a first insulating film in order to decrease a parasitic capacitance between gate line and a substrate. For example, in FINFET (IEDM 2010 CC. Wu, et. al., 27.1.1-27.1.4.), a first insulating film is formed around a fin-shaped semiconductor layer and then etched back to expose the fin-shaped semiconductor layer, thereby decreasing the parasitic capacitance between the gate line and the substrate. Also, in SGT, the first insulating film must be used for decreasing the parasitic capacitance between the gate line and the substrate. The SGT includes the pillar-shaped semiconductor layer in addition to the fin-shaped semiconductor layer, and thus some consideration is required for forming the pillar-shaped semiconductor layer.

On the other hand, FIN FET has been known, in which two transistors are formed from one dummy pattern (for example, Japanese Unexamined Patent Application Publication No. 2011-71235). A sidewall is formed around the dummy pattern and used as a mask for etching a substrate to form a fin, thereby forming two transistors from one dummy pattern.

Since the two transistors are formed, one of the transistors can be used as an nMOS transistor and the other one can be used a pMOS transistor.

SUMMARY

Accordingly, an object is to decrease a parasitic capacitance between a gate line and a substrate, provide a CMOS SGT manufacturing method for forming nMOS SGT and pMOS SGT from one dummy pattern using a gate last process, and provide a resulting SGT structure.

Solution to Problem

A method for manufacturing a semiconductor device of the present invention includes: a first step of forming a first fin-shaped silicon layer and a second fin-shaped silicon layer on a substrate so that the first fin-shaped silicon layer and the second fin-shaped silicon layer are connected to each other at the ends thereof to form a closed loop, forming a first insulating film around the first fin-shaped silicon layer and the second fin-shaped silicon layer, forming a first pillar-shaped silicon layer on the first fin-shaped silicon layer, and forming a second pillar-shaped silicon layer on the second fin-shaped silicon layer, the width of the first pillar-shaped silicon layer being equal to the width of the first fin-shaped silicon layer and the width of the second pillar-shaped silicon layer being equal to the width of the second fin-shaped silicon layer; a second step of, after the first step, forming n-type diffusion layers by implanting impurities in an upper portion of the first pillar-shaped silicon layer, an upper portion of the first fin-shaped silicon layer, and a lower portion of the first pillar-shaped silicon layer and forming p-type diffusion layers by implanting impurities in an upper portion of the second pillar-shaped silicon layer, an upper portion of the second fin-shaped silicon layer, and a lower portion of the second pillar-shaped silicon layer; a third step of, after the second step, forming a gate insulating film, a first polysilicon gate electrode, a second polysilicon gate electrode, and a polysilicon gate line so that the gate insulating film covers the peripheries and the tops of the first pillar-shaped silicon layer and the second pillar-shaped silicon layer, the first polysilicon gate electrode and the second polysilicon gate electrode cover the gate insulating film, and after the first polysilicon gate electrode, the second polysilicon gate electrode, and the polysilicon gate line are formed, the top position of polysilicon is higher than the gate insulating film on the n-type diffusion layer formed in the upper portion of the first pillar-shaped silicon layer and higher than the gate insulating film on the p-type diffusion layer formed in the upper portion of the second pillar-shaped silicon layer; a fourth step of, after the third step, forming a silicide in an upper portion of the n-type diffusion layer in the upper portion of the first fin-shaped silicon layer and in an upper portion of the p-type diffusion layer in the upper portion of the second fin-shaped silicon layer; a fifth step of, after the fourth step, depositing an interlayer insulating film, exposing the first polysilicon gate electrode, the second polysilicon gate electrode, and the polysilicon gate line, etching the first polysilicon gate electrode, the second polysilicon gate electrode, and the polysilicon gate line, and then depositing a metal to form a first metal gate electrode, a second metal gate electrode, and a metal gate line, the metal gate line being connected to the first metal gate electrode and the second metal gate electrode and extending in a direction perpendicular to the first fin-shaped silicon layer and the second fin-shaped silicon layer; and a sixth step of, after the fifth step, forming a first contact and a second contact so that the first contact is in direct contact with the n-type diffusion layer in the upper portion of the first pillar-shaped silicon layer and the second contact is in direct contact with the p-type diffusion layer in the upper portion of the second pillar-shaped silicon layer.

The manufacturing method is also characterized in that in the first step, a second oxide film is deposited for forming a dummy pattern on the substrate, a first resist is formed for forming the dummy pattern, the second oxide film is etched to form the dummy pattern, the first resist is removed, a first nitride film is deposited and then etched to be left as a sidewall and to form a first nitride film sidewall around the dummy pattern, the dummy pattern is removed, the silicon substrate is etched using the first nitride film sidewall as a mask to form the first fin-shaped silicon layer and the second fin-shaped silicon layer which are connected to each other at the ends to form a closed loop, the first insulating film is formed around the first fin-shaped silicon layer and the second fin-shaped silicon layer, the first nitride film sidewall is removed, the first insulating film is etched back to expose upper portions of the first fin-shaped silicon layer and the second fin-shaped silicon layer, a second resist is formed to be perpendicular to the first fin-shaped silicon layer and the second fin-shaped silicon layer, the first fin-shaped silicon layer and the second fin-shaped silicon layer are etched, and the second resist is removed to form the first pillar-shaped silicon layer so that a portion where the first fin-shaped silicon layer and the second resist intersect at right angles becomes the first pillar-shaped silicon layer and form the second pillar-shaped silicon layer so that a portion where the second fin-shaped silicon layer and the second resist intersect at right angles becomes the second pillar-shaped silicon layer.

The manufacturing method is further characterized in that in the second step after the first step, in the whole structure after the first step, a third oxide film is deposited, a second nitride film is formed and then etched to be left as a sidewall, a third resist is formed for forming the n-type diffusion layers, impurities are implanted to form the n-type diffusion layers in an upper portion of the first pillar-shaped silicon layer and an upper portion of the first fin-shaped silicon layer, the third resist is removed, the second nitride film and the third oxide film are removed, heat treatment is performed, a fourth oxide film is deposited, a third nitride film is formed and then etched to be left as a sidewall, a fourth resist is formed for forming the p-type diffusion layers, impurities are implanted to form the p-type diffusion layers in an upper portion of the second pillar-shaped silicon layer and an upper portion of the second fin-shaped silicon layer, the fourth resist is removed, the fourth oxide film and the third nitride film are removed, and heat treatment is performed.

The manufacturing method is further characterized in that in the third step after the second step, the gate insulating film is formed to surround the pillar-shaped silicon layers, polysilicon is deposited and then planarized so that after planarization, the top surface of the polysilicon is higher than the gate insulating film on the n-type diffusion layer formed in the upper portion of the first pillar-shaped silicon layer and higher than the gate insulating film on the p-type diffusion layer formed in the upper portion of the second pillar-shaped silicon layer, a fourth nitride film is deposited, a fifth resist is formed for forming the first polysilicon gate electrode, the second polysilicon gate electrode, and the polysilicon gate line, the fourth nitride film is etched, the polysilicon is etched to form the first polysilicon gate electrode, the second polysilicon gate electrode, and the polysilicon gate line, the gate insulating films are etched, and the fifth resist is removed.

The manufacturing method is further characterized in that in the fourth step, in the whole structure after the third step, a fifth nitride film is deposited and then etched to be left as a sidewall, and a metal is deposited to form silicides in upper portions of the n-type diffusion layer and the p-type diffusion layer in the upper portions of the first fin-shaped silicon layer and the second fin-shaped silicon layer, respectively.

The manufacturing method is further characterized in that in the fifth step, in the whole structure after the fourth step, a sixth nitride film is deposited, the interlayer insulating film is deposited and then planarized by chemical mechanical polishing, the first polysilicon gate electrode, the second polysilicon gate electrode, and the polysilicon gate line are exposed by chemical mechanical polishing, the first polysilicon gate electrode, the second polysilicon gate electrode, and the polysilicon gate line are etched, a metal is deposited to be filled in portions from which the first polysilicon gate electrode, the second polysilicon gate electrode, and the polysilicon gate line have been removed, and the metal is etched to expose the gate insulating film on the n-type diffusion layer in the upper portion of the first pillar-shaped silicon layer and expose the gate insulating film on the p-type diffusion layer in the upper portion of the second pillar-shaped silicon layer, thereby forming the first metal gate electrode, the second metal gate electrode, and the metal gate line.

A semiconductor device according to an embodiment includes a first fin-shaped semiconductor layer on a substrate and a second fin-shaped semiconductor layer on the substrate, where the first fin-shaped semiconductor layer and the second fin-shaped semiconductor layer correspond to the dimensions of a sidewall pattern around a dummy pattern. A first insulating film resides around the first fin-shaped semiconductor layer and the second fin-shaped semiconductor layer. A first pillar-shaped semiconductor layer resides on the first fin-shaped semiconductor layer and a second pillar-shaped semiconductor layer resides on the second fin-shaped semiconductor layer. An n-type diffusion layer is in an upper portion of the first fin-shaped semiconductor layer and a lower portion of the first pillar-shaped semiconductor layer. An n-type diffusion layer is in an upper portion of the first pillar-shaped semiconductor layer. A p-type diffusion layer is in an upper portion of the second fin-shaped semiconductor layer and a lower portion of the second pillar-shaped semiconductor layer. A p-type diffusion layer is in an upper portion of the second pillar-shaped semiconductor layer. A first gate insulating film resides around the first pillar-shaped semiconductor layer, a first metal gate electrode resides around the gate insulating film. A second gate insulating film resides around the second pillar-shaped semiconductor layer and a second metal gate electrode resides around the gate insulating film. A metal gate line is connected to the first metal gate electrode and the second metal gate electrode and extends in a direction perpendicular to the first fin-shaped semiconductor layer and the second fin-shaped semiconductor layer.

According to the present invention, it is possible to decrease a parasitic capacitance between a gate line and a substrate, provide a CMOS SGT manufacturing method for forming nMOS SGT and pMOS SGT from one dummy pattern using a gate last process, and provide a resulting SGT structure. The manufacturing method is based on a conventional FINFET manufacturing method in which a sidewall is formed around a dummy pattern and used as a mask for etching a substrate to form a fin, thereby forming two transistors from one dummy pattern, and thus two SGTs can be easily formed from one dummy pattern.

Since the two SGTs including one serving as nMOS SGT and the other one serving as pMOS SGT are formed, one CMOS SGT can be formed from one dummy pattern, and thus CMOS SGT with high integration can be provided.

In addition, a silicide is generally formed in an upper portion of a pillar-shaped silicon layer, but a silicide must be formed after a polysilicon gate is formed because the deposition temperature of polysilicon is higher than the silicide formation temperature. Therefore, when the silicide is formed in an upper portion of a silicon column, a hole is formed on a polysilicon gate electrode after the polysilicon gate is formed, the silicide is formed after a sidewall composed of an insulating film is formed on the sidewall of the hole, and then the hole is filled with an insulating film, thereby causing the problem of increasing the number of manufacturing steps. Therefore, the diffusion layers are formed before the polysilicon gate electrode and the polysilicon gate line are formed, the pillar-shaped silicon layer is covered with the polysilicon gate electrode, and the silicide is formed only in an upper portion of the fin-shaped silicon layer. Therefore, a usual metal gate last manufacturing method can be used, in which a gate is formed using polysilicon, the interlayer insulating film is deposited, the polysilicon gate is exposed by chemical mechanical polishing and then etched, and then a metal is deposited, thereby facilitating the formation of metal gate CMOS SGT.

BRIEF DESCRIPTION OF THE DRAWING

FIG. **1**A is a plan view of a semiconductor device according to the present invention, FIG. **1**B is a sectional view taken along line X-X' in FIG. **1**A, and FIG. **1**C is a sectional view taken along line Y-Y' in FIG. **1**A.

FIG. **2**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **2**B is a sectional view taken along line X-X' in FIG. **2**A, and FIG. **2**C is a sectional view taken along line Y-Y' in FIG. **2**A.

FIG. **3**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **3**B is a sectional view taken along line X-X' in FIG. **3**A, and FIG. **3**C is a sectional view taken along line Y-Y' in FIG. **3**A.

FIG. **4**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **4**B is a sectional view taken along line X-X' in FIG. **4**A, and FIG. **4**C is a sectional view taken along line Y-Y' in FIG. **4**A.

FIG. **5**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **5**B is a sectional view taken along line X-X' in FIG. **5**A, and FIG. **5**C is a sectional view taken along line Y-Y' in FIG. **5**A.

FIG. **6**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **6**B is a sectional view taken along line X-X' in FIG. **6**A, and FIG. **6**C is a sectional view taken along line Y-Y' in FIG. **6**A.

FIG. **7**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **7**B is a sectional view taken along line X-X' in FIG. **7**A, and FIG. **7**C is a sectional view taken along line Y-Y' in FIG. **7**A.

FIG. **8**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **8**B is a sectional view taken along line X-X' in FIG. **8**A, and FIG. **8**C is a sectional view taken along line Y-Y' in FIG. **8**A.

FIG. **9**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **9**B is a sectional view taken along line X-X' in FIG. **9**A, and FIG. **9**C is a sectional view taken along line Y-Y' in FIG. **9**A.

FIG. **10**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **10**B is a sectional view taken along line X-X' in FIG. **10**A, and FIG. **10**C is a sectional view taken along line Y-Y' in FIG. **10**A.

FIG. **11**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **11**B is a sectional view taken along line X-X' in FIG. **11**A, and FIG. **11**C is a sectional view taken along line Y-Y' in FIG. **11**A.

FIG. **12**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **12**B is a sectional view taken along line X-X' in FIG. **12**A, and FIG. **12**C is a sectional view taken along line Y-Y' in FIG. **12**A.

FIG. **13**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **13**B is a sectional view taken along line X-X' in FIG. **13**A, and FIG. **13**C is a sectional view taken along line Y-Y' in FIG. **13**A.

FIG. **14**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **14**B is a sectional view taken along line X-X' in FIG. **14**A, and FIG. **14**C is a sectional view taken along line Y-Y' in FIG. **14**A.

FIG. **15**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **15**B is a sectional view taken along line X-X' in FIG. **15**A, and FIG. **15**C is a sectional view taken along line Y-Y' in FIG. **15**A.

FIG. **16**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **16**B is a sectional view taken along line X-X' in FIG. **16**A, and FIG. **16**C is a sectional view taken along line Y-Y' in FIG. **16**A.

FIG. **17**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **17**B is a sectional view taken along line X-X' in FIG. **17**A, and FIG. **17**C is a sectional view taken along line Y-Y' in FIG. **17**A.

FIG. **18**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **18**B is a sectional view taken along line X-X' in FIG. **18**A, and FIG. **18**C is a sectional view taken along line Y-Y' in FIG. **18**A.

FIG. **19**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **19**B is a sectional view taken along line X-X' in FIG. **19**A, and FIG. **19**C is a sectional view taken along line Y-Y' in FIG. **19**A.

FIG. **20**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **20**B is a sectional view taken along line X-X' in FIG. **20**A, and FIG. **20**C is a sectional view taken along line Y-Y' in FIG. **20**A.

FIG. **21**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **21**B is a sectional view taken along line X-X' in FIG. **21**A, and FIG. **21**C is a sectional view taken along line Y-Y' in FIG. **21**A.

FIG. **22**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **22**B is a sectional view taken along line X-X' in FIG. **22**A, and FIG. **22**C is a sectional view taken along line Y-Y' in FIG. **22**A.

FIG. **23**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **23**B is a sectional view taken along line X-X' in FIG. **23**A, and FIG. **23**C is a sectional view taken along line Y-Y' in FIG. **23**A.

FIG. **24**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **24**B is a sectional view taken along line X-X' in FIG. **24**A, and FIG. **24**C is a sectional view taken along line Y-Y' in FIG. **24**A.

FIG. **25**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **25**B is a sectional view taken along line X-X' in FIG. **25**A, and FIG. **25**C is a sectional view taken along line Y-Y' in FIG. **25**A.

FIG. **26**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **26**B is a sectional view taken along line X-X' in FIG. **26**A, and FIG. **26**C is a sectional view taken along line Y-Y' in FIG. **26**A.

FIG. **27**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **27**B is a sectional view taken along line X-X' in FIG. **27**A, and FIG. **27**C is a sectional view taken along line Y-Y' in FIG. **27**A.

FIG. **28**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **28**B is a sectional view taken along line X-X' in FIG. **28**A, and FIG. **28**C is a sectional view taken along line Y-Y' in FIG. **28**A.

FIG. **29**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **29**B is a sectional view taken along line X-X' in FIG. **29**A, and FIG. **29**C is a sectional view taken along line Y-Y' in FIG. **29**A.

FIG. **30**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **30**B is a sectional view taken along line X-X' in FIG. **30**A, and FIG. **30**C is a sectional view taken along line Y-Y' in FIG. **30**A.

FIG. **31**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **31**B is a sectional view taken along line X-X' in FIG. **31**A, and FIG. **31**C is a sectional view taken along line Y-Y' in FIG. **31**A.

FIG. **32**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **32**B is a sectional view taken along line X-X' in FIG. **32**A, and FIG. **32**C is a sectional view taken along line Y-Y' in FIG. **32**A.

FIG. **33**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **33**B is a sectional view taken along line X-X' in FIG. **33**A, and FIG. **33**C is a sectional view taken along line Y-Y' in FIG. **33**A.

FIG. **34**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **34**B is a sectional view taken along line X-X' in FIG. **34**A, and FIG. **34**C is a sectional view taken along line Y-Y' in FIG. **34**A.

FIG. **35**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **35**B is a sectional view taken along line X-X' in FIG. **35**A, and FIG. **35**C is a sectional view taken along line Y-Y' in FIG. **35**A.

FIG. **36**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **36**B is a sectional view taken along line X-X' in FIG. **36**A, and FIG. **36**C is a sectional view taken along line Y-Y' in FIG. **36**A.

FIG. **37**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **37**B is a sectional view taken along line X-X' in FIG. **37**A, and FIG. **37**C is a sectional view taken along line Y-Y' in FIG. **37**A.

FIG. **38**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **38**B is a sectional view taken along line X-X' in FIG. **38**A, and FIG. **38**C is a sectional view taken along line Y-Y' in FIG. **38**A.

FIG. **39**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **39**B is a sectional view taken along line X-X' in FIG. **39**A, and FIG. **39**C is a sectional view taken along line Y-Y' in FIG. **39**A.

FIG. **40**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **40**B is a sectional view taken along line X-X' in FIG. **40**A, and FIG. **40**C is a sectional view taken along line Y-Y' in FIG. **40**A.

FIG. **41**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **41**B is a sectional view taken along line X-X' in FIG. **41**A, and FIG. **41**C is a sectional view taken along line Y-Y' in FIG. **41**A.

FIG. **42**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **42**B is a sectional view taken along line X-X' in FIG. **42**A, and FIG. **42**C is a sectional view taken along line Y-Y' in FIG. **42**A.

FIG. **43**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **43**B is a sectional view taken along line X-X' in FIG. **43**A, and FIG. **43**C is a sectional view taken along line Y-Y' in FIG. **43**A.

FIG. **44**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **44**B is a sectional view taken along line X-X' in FIG. **44**A, and FIG. **44**C is a sectional view taken along line Y-Y' in FIG. **44**A.

FIG. **45**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **45**B is a sectional view taken along line X-X' in FIG. **45**A, and FIG. **45**C is a sectional view taken along line Y-Y' in FIG. **45**A.

FIG. **46**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **46**B is a sectional view taken along line X-X' in FIG. **46**A, and FIG. **46**C is a sectional view taken along line Y-Y' in FIG. **46**A.

FIG. **47**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **47**B is a sectional view taken along line X-X' in FIG. **47**A, and FIG. **47**C is a sectional view taken along line Y-Y' in FIG. **47**A.

FIG. **48**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **48**B is a sectional view taken along line X-X' in FIG. **48**A, and FIG. **48**C is a sectional view taken along line Y-Y' in FIG. **48**A.

FIG. **49**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **49**B is a sectional view taken along line X-X' in FIG. **49**A, and FIG. **49**C is a sectional view taken along line Y-Y' in FIG. **49**A.

FIG. **50**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **50**B is a sectional view taken along line X-X' in FIG. **50**A, and FIG. **50**C is a sectional view taken along line Y-Y' in FIG. **50**A.

FIG. **51**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **51**B is a sectional view taken along line X-X' in FIG. **51**A, and FIG. **51**C is a sectional view taken along line Y-Y' in FIG. **51**A.

FIG. **52**A is a plan view of a method for manufacturing a semiconductor device according to the present invention, FIG. **52**B is a sectional view taken along line X-X' in FIG. **52**A, and FIG. **52**C is a sectional view taken along line Y-Y' in FIG. **52**A.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A manufacturing process for forming a SGT structure according to an embodiment of the present invention is described below with reference to FIGS. **2** to **52**.

A description is given of a manufacturing method for forming a first fin-shaped silicon layer and a second fin-shaped silicon layer on a substrate, forming a first insulating film around the first fin-shaped silicon layer and the second fin-shaped silicon layer, and forming a first pillar-shaped silicon layer on the first fin-shaped silicon layer and forming a second pillar-shaped silicon layer on the second fin-shaped silicon layer.

As shown in FIGS. **2**A-**2**C, a second oxide film **102** is formed for forming a dummy pattern on a silicon substrate **101**. A nitride film or a laminated film of an oxide film and polysilicon may be used.

As shown in FIGS. **3**A-**3**C, a first resist **103** is formed for forming the dummy pattern.

As shown in FIGS. **4**A-**4**C, the second oxide film **102** is etched to form the dummy pattern **102**.

As shown in FIGS. **5**A-**5**C, the first resist **103** is removed.

As shown in FIGS. **6**A-**6**C, a first nitride film **104** is deposited.

As shown in FIGS. **7**A-**7**C, the first nitride film **104** is etched to be left as a sidewall. Consequently, a first nitride film sidewall **104** is formed around the dummy pattern **102**. The first nitride film sidewall **104** is used for etching silicon to form a first fin-shaped silicon layer **106** and a second fin-shaped silicon layer **105** which are connected to each other at the ends thereof to form a closed loop.

As shown in FIGS. **8**A-**8**C, the dummy pattern **102** is removed.

As shown in FIGS. **9**A-**9**C, the silicon substrate **101** is etched using the first nitride film sidewall **104** as a mask to form the first fin-shaped silicon layer **106** and the second fin-shaped silicon layer **105** which are connected to each other at the ends thereof to form a closed loop.

As shown in FIGS. **10**A-**10**C, a first insulating film **107** is formed around the first fin-shaped silicon layer **106** and the second fin-shaped silicon layer **105**. As the first insulating film, an oxide film formed by high-density plasma, or an oxide film formed by low-pressure chemical vapor deposition may be used.

As shown in FIGS. **11**A-**11**C, the first nitride film sidewall **104** is removed. When the first nitride film sidewall **104** is removed during silicon etching or deposition of the oxide film, this step is not required.

As shown in FIGS. **12**A-**12**C, the first insulating film **107** is etched back to expose an upper portion of the first fin-shaped silicon layer **106** and an upper portion of the second fin-shaped silicon layer **105**.

As shown in FIGS. **13**A-**13**C, a second resist **108** is formed so as to be perpendicular to the first fin-shaped silicon layer **106** and the second fin-shaped silicon layer **105**. A portion where each of the first fin-shaped silicon layer **106** and the second fin-shaped silicon layer **105** intersects at right angles the second resist **108** becomes a pillar-shaped silicon layer. Since a linear resist can be used, the resist is unlikely to fall after patterning, thereby realizing a stable process.

As shown in FIGS. **14**A-**14**C, the first fin-shaped silicon layer **106** and the second fin-shaped silicon layer are etched. A portion where the first fin-shaped silicon layer **106** and the second resist **108** intersect at right angles becomes a first pillar-shaped silicon layer **110**. A portion where the second fin-shaped silicon layer **105** and the second resist **108** intersect at right angles becomes a second pillar-shaped silicon layer **109**. Therefore, the width of the first pillar-shaped silicon layer **110** is equal to the width of the first fin-shaped silicon layer **106**. Also, the width of the second pillar-shaped silicon layer **109** is equal to the width of the second fin-shaped silicon layer **105**.

As a result, a structure is formed, in which the first pillar-shaped silicon layer **110** is formed in an upper portion of the first fin-shaped silicon layer **106**, the second pillar-shaped silicon layer **109** is formed in an upper portion of the second fin-shaped silicon layer **105**, and the first insulating film **107** is formed around the first fin-shaped silicon layer **106** and the second fin-shaped silicon layer **105**.

As shown in FIGS. **15**A-**16**C, the second resist **108** is removed.

Next, a description is given of a manufacturing method in which in order to use a gate-last process, n-type diffusion layers are formed by implanting impurities in an upper portion of the first pillar-shaped silicon layer **110**, an upper portion of the first fin-shaped silicon layer **106**, and a lower portion of the first pillar-shaped silicon layer **110**, and p-type diffusion layers are formed by implanting impurities in an upper portion of the second pillar-shaped silicon layer **109**, an upper portion of the second fin-shaped silicon layer **105**, and a lower portion of the second pillar-shaped silicon layer **109**.

As shown in FIGS. **16**A-**16**C, a third oxide film **111** is deposited, and a second nitride film **112** is formed. Since upper portions of the pillar-shaped silicon layers are subsequently covered with a gate insulating film and polysilicon gate electrodes, diffusion layers are formed in upper portions of the pillar-shaped silicon layers before covering of the pillar-shaped silicon layers.

As shown in FIGS. **17**A-**17**C, the second nitride film **112** is etched to be left as a sidewall.

As shown in FIGS. **18**A-**18**C, a third resist **113** is formed for forming the n-type diffusion layers by impurity implantation in an upper portion of the first pillar-shaped silicon layer **110**, an upper portion of the first fin-shaped silicon layer **106**, and a lower portion of the first pillar-shaped silicon layer **110**.

As shown in FIGS. **19**A-**19**C, impurities such as arsenic or phosphorus are implanted to form a n-type diffusion layer **115** in an upper portion of the first pillar-shaped silicon layer **110**, and n-type diffusion layers **116** and **117** in an upper portion of the first fin-shaped silicon layer **106**.

As shown in FIGS. **20**A-**20**C, the third resist **113** is removed.

As shown in FIGS. **21**A-**21**C, the second nitride film **112** and the third oxide film **111** are removed.

As shown in FIGS. **22**A-**22**C, heat treatment is performed. The n-type diffusion layers **116** and **117** in an upper portion of the first fin-shaped silicon layer **106** are brought into contact with each other to form a n-type diffusion layer **118**.

As shown in FIGS. **23**A-**23**C, a fourth oxide film **119** is deposited, and a third nitride film **120** is formed. Since upper portions of the pillar-shaped silicon layers are subsequently covered with a gate insulating film and polysilicon gate electrodes, diffusion layers are formed in upper portions of the pillar-shaped silicon layers before the pillar-shaped silicon layers are covered.

As shown in FIGS. **24**A-**24**C, the third nitride film **120** is etched to be left as a sidewall.

As shown in FIGS. **25**A-**25**C, a fourth resist **121** is formed for forming the p-type diffusion layers by impurity implantation in an upper portion of the second pillar-shaped silicon layer **109**, an upper portion of the second fin-shaped silicon layer **105**, and a lower portion of the second pillar-shaped silicon layer **109**.

As shown in FIGS. **26**A-**26**C, impurities such as boron are implanted to form a p-type diffusion layer **122** in an upper portion of the second pillar-shaped silicon layer **109**, and p-type diffusion layers **123** and **124** in an upper portion of the second fin-shaped silicon layer **105**.

As shown in FIGS. **27**A-**27**C, the fourth resist **121** is removed.

As shown in FIGS. **28**A-**28**C, the third nitride film **120** and the fourth oxide film **119** are removed.

As shown in FIGS. **29**A-**29**C, heat treatment is performed. The p-type diffusion layers **123** and **124** in an upper portion of the second fin-shaped silicon layer **105** are brought into contact with each other to form a n-type diffusion layer **125**.

As described above, in order to use the gate-last process, the n-type diffusion layers **115** and **118** are formed by impurity implantation in an upper portion of the first pillar-shaped silicon layer **110** and in an upper portion of the first fin-shaped silicon layer **106** and a lower portion of the first pillar-shaped silicon layer **110**, and the p-type diffusion layers **122** and **125** are formed by impurity implantation in an upper portion of the second pillar-shaped silicon layer **109** and in an upper portion of the second fin-shaped silicon layer **105** and a lower portion of the second pillar-shaped silicon layer **109**.

Since nMOS SGT and pMOS SGT can be formed as described above, a CMOS SGT can be formed from one dummy pattern.

In addition, when the line width of the dummy pattern is minimum feature size F, the distance between the first pillar-shaped silicon layer **110** and the second pillar-shaped silicon layer **109** is the minimum feature size F. Therefore, an allowance for alignment of a resist mask for impurity implantation can be made F/2, thereby making it easy to separate between pMOS and nMOS elements.

Next, a description is given of a manufacturing method for forming a first polysilicon gate electrode **127***a*, a second polysilicon gate electrode **127***b*, and a polysilicon gate line **127***c* using polysilicon in order to use the gate-last process. In order to use the gate-last process, an interlayer insulating film is deposited, and then the polysilicon gate electrodes and the polysilicon gate line are exposed by chemical mechanical polishing. Therefore, it is necessary to prevent upper portions of the pillar-shaped silicon layers from being exposed by chemical mechanical polishing.

As shown in FIGS. **30**A-**30**C, a gate insulating film **126** is formed, and polysilicon **127** is deposited and then planarized. After planarization, the top position of the polysilicon **127** is higher than the gate insulating film **126** disposed on the n-type diffusion layer **115** in an upper portion of the first pillar-shaped silicon layer **110** and higher than the gate insulating film **126** disposed on the p-type diffusion layer **122** in an upper portion of the second pillar-shaped silicon layer **109**. As a result, when in order to use the gate-last process, the polysilicon gate electrodes and the polysilicon gate line are exposed by chemical mechanical polishing after the interlayer insulating film is deposited, the upper portions of the pillar-shaped silicon layers are not exposed by chemical mechanical polishing.

In addition, a fourth nitride film **128** is deposited. The fourth nitride film **128** is a film which inhibits the formation of silicide in upper portions of the first polysilicon gate electrode **127***a*, the second polysilicon gate electrode **127***b*, and the polysilicon gate line **127***c* when the silicide is formed in upper portions of the first fin-shaped silicon layer **106** and the second fin-shaped silicon layer **105**.

As shown in FIGS. **31**A-**31**C, a fifth resist **129** is formed for forming the first polysilicon gate electrode **127***a*, the second polysilicon gate electrode **127***b*, and the polysilicon gate line **127***c*. A portion corresponding to the gate line is preferably perpendicular to the first fin-shaped silicon layer **106** and the second fin-shaped silicon layer **105**. This is because a parasitic capacitance between the gate line and the substrate is decreased.

As shown in FIGS. **32**A-**32**C, the fourth nitride film **128** is etched, and the polysilicon **127** is etched to form the first polysilicon gate electrode **127***a*, the second polysilicon gate electrode **127***b*, and the polysilicon gate line **127***c*.

As shown in FIGS. **33**A-**33**C, the gate insulating film **126** is etched.

As shown in FIGS. **34**A-**34**C, the fifth resist **129** is removed.

The manufacturing method for forming, using polysilicon, the first polysilicon gate electrode **127***a*, the second polysilicon gate electrode **127***b*, and the polysilicon gate line **127***c* in order to use the gate-last process is described above. After the first polysilicon gate electrode **127***a*, the second polysilicon gate electrode **127***b*, and the polysilicon gate line **127***c* are formed, the top position of polysilicon is higher than the gate insulating film **126** on the n-type diffusion layer **115** in an upper portion of the first pillar-shaped silicon layer **110** and higher than the gate insulating film **126** on the p-type diffusion layer **122** in an upper portion of the second pillar-shaped silicon layer **109**.

Next, a manufacturing method for forming silicides in an upper portion of the n-type diffusion layer **118** formed in an upper portion of the first fin-shaped silicon layer **106** and in an upper portion of the p-type diffusion layer **125** formed in an upper portion of the second fin-shaped silicon layer **105** is described.

A silicide is not formed in upper portions of the first polysilicon gate electrode **127***a*, the second polysilicon gate electrode **127***b*, and the polysilicon gate line **127***c*, in the n-type diffusion layer **115** in an upper portion of the first pillar-shaped silicon layer **110**, and in the p-type diffusion layer **122** in an upper portion of the second pillar-shaped silicon layer **109**. When the silicide is formed in the n-type diffusion layer **115** in an upper portion of the first pillar-shaped silicon layer **110**, and in the p-type diffusion layer **122** in an upper portion of the second pillar-shaped silicon layer **109**, the manufacturing process is enlarged.

As shown in FIGS. **35**A-**35**C, a fifth nitride film **130** is deposited.

As shown in FIGS. **36**A-**36**C, the fifth nitride film **130** is etched to be left as a sidewall.

As shown in FIGS. **37**A-**37**C, a metal such as nickel or cobalt is deposited to form silicide **131** in upper portions of the n-type diffusion layer **118** and the p-type diffusion layer **125** formed in upper portions of the first fin-shaped silicon layer **106** and the second fin-shaped silicon layer **105**, respectively. At this time, the first polysilicon gate electrode **127***a*, the second polysilicon gate electrode **127***b*, and the polysilicon gate line **127***c* are covered with the fifth nitride film **130** and the fourth nitride film **128**, and the n-type diffusion layer **115** in an upper portion of the first pillar-shaped silicon layer **110** and the p-type diffusion layer **122** in an upper portion of the second pillar-shaped silicon layer **109** are covered with the gate insulating film **126**, the first polysilicon gate electrode **127***a*, the second polysilicon gate electrode **127***b*, and the polysilicon gate line **127***c*, and thus a silicide is not formed in these portions.

The manufacturing method for forming a silicide in an upper portion of the n-type diffusion layer **118** in an upper portion of the first fin-shaped silicon layer **106** and in an upper portion of the p-type diffusion layer **125** in an upper portion of the second fin-shaped silicon layer **105** is described above.

Next, a gate-last manufacturing method is described, in which after an interlayer insulting film **133** is deposited, the first polysilicon gate electrode **127***a*, the second polysilicon gate electrode **127***b*, and the polysilicon gate line **127***c* are exposed, the first polysilicon gate electrode **127***a*, the second polysilicon gate electrode **127***b*, and the polysilicon gate line **127***c* are etched, and then a metal is deposited to form a first metal gate electrode **134***a*, a second metal gate electrode **134***b*, and a metal gate line **134***c*.

As shown in FIGS. **38**A-**38**C, a sixth nitride film **132** is deposited for protecting the silicide **131**.

As shown in FIGS. **39**A-**39**C, an interlayer insulating film **133** is deposited and then planarized by chemical mechanical polishing.

As shown in FIGS. **40**A-**40**C, the first polysilicon gate electrode **127***a*, the second polysilicon gate electrode **127***b*, and the polysilicon gate line **127***c* are exposed by chemical mechanical polishing.

As shown in FIGS. **41**A-**41**C, the first polysilicon gate electrode **127***a*, the second polysilicon gate electrode **127***b*, and the polysilicon gate line **127***c* are etched. Wet etching is preferred.

As shown in FIGS. **42**A-**42**C, a metal **134** is deposited and then planarized to fill, with the metal **134**, portions from which the first polysilicon gate electrode **127***a*, the second polysilicon gate electrode **127***b*, and the polysilicon gate line **127***c* have been removed. Atomic layer deposition is preferably used.

As shown in FIGS. **43**A-**43**C, the metal **134** is etched to expose the gate insulating film **126** formed on the n-type diffusion layer **115** in an upper portion of the first pillar-shaped silicon layer **110** and expose the gate insulating film **126** formed on the p-type diffusion layer **122** in an upper portion of the second pillar-shaped silicon layer **109**. Consequently, the first metal gate electrode **134***a*, the second metal gate electrode **134***b*, and the metal gate line **134***c* are formed.

The gate-last manufacturing method is described above, in which after the interlayer insulating film **133** is deposited, the first polysilicon gate electrode **127***a*, the second polysilicon gate electrode **127***b*, and the polysilicon gate line **127***c* are exposed, the first polysilicon gate electrode **127***a*, the second polysilicon gate electrode **127***b*, and the polysilicon gate line **127***c* are etched, and then the metal **134** is deposited to form the first metal gate electrode **134***a*, the second metal gate electrode **134***b*, and the metal gate line **134***c*.

Next, a manufacturing method for forming a contact is described. Since a silicide is not formed in the n-type diffusion layer **115** in an upper portion of the first pillar-shaped silicon layer **110** and in the p-type diffusion layer **122** in an upper portion of the second pillar-shaped silicon layer **109**, a first contact is brought into direct contact with the n-type diffusion layer **115** in an upper portion of the first pillar-shaped silicon layer **110** and a second contact is brought into direct contact with the p-type diffusion layer **122** in an upper portion of the second pillar-shaped silicon layer **109**.

As shown in FIGS. **44**A-**44**C, an interlayer insulating film **135** is deposited and then planarized.

As shown in FIGS. **45**A-**45**C, a sixth resist **136** is formed for forming a first contact hole **138** on the first pillar-shaped silicon layer **110** and a second contact hole **137** on the second pillar-shaped silicon layer **109**. Then, the interlayer insulating film **135** is etched to form the first contact hole **138** and the second contact hole **137**.

As shown in FIGS. **46**A-**46**C, the sixth resist **136** is removed.

As shown in FIGS. **47**A-**47**C, a seventh resist **139** is formed for forming a third contact hole **140** and a fourth contact hole **141** on the metal gate line **134***c* and on the first fin-shaped silicon layer **106** and the second fin-shaped silicon layer **105**.

As shown in FIGS. **48**A-**48**C, the interlayer insulating films **135** and **133** are etched to form the third contact hole **140** and the fourth contact hole **141**.

As shown in FIGS. **49**A-**49**C, the seventh resist **139** is removed, and the sixth nitride film **132** and the gate insulating film **126** are etched to expose the silicide **131**, the n-type diffusion layer **115**, and the p-type diffusion layer **122**. Then, a metal is deposited to form a first contact **144**, a second contact **143**, a third contact **142**, and a fourth contact **145**.

The manufacturing method for forming contacts is described above. Since a silicide is not formed in the n-type diffusion layer **115** in an upper portion of the first pillar-shaped silicon layer **110** and in the p-type diffusion layer **122** in an upper portion of the second pillar-shaped silicon layer **109**, the first contact is brought into direct contact with the n-type diffusion layer **115** in an upper portion of the first pillar-shaped silicon layer **110**, and the second contact is brought into direct contact with the p-type diffusion layer **122** in an upper portion of the second pillar-shaped silicon layer **109**.

Next, a manufacturing method for forming a metal wiring layer is described.

As shown in FIGS. **50**A-**50**C, a metal **146** is deposited.

As shown in FIGS. **51**A-**51**C, eighth resists **147**, **148**, **149**, and **150** are formed for forming the metal wiring, and the metal **146** is etched to form metal wirings **151**, **152**, **153**, and **154**.

As shown in FIGS. **52**A-**52**C, the eighth resists **147**, **148**, **149**, and **150** are removed.

The manufacturing method for forming metal wiring layers is described above.

The result of the above-described manufacturing method is shown in FIGS. **1**A-**1**C.

The resulting structure includes: the first fin-shaped silicon layer **106** formed on the substrate **101** and the second silicon layer **105** formed on the substrate **101**, the first fin-shaped silicon layer **106** and the second fin-shaped silicon layer **105** being connected to each other at the ends thereof to form a closed loop; the first insulating film **107** formed around the first fin-shaped silicon layer **106** and the second fin-shaped silicon layer **105**; the first pillar-shaped silicon layer **110** formed on the first fin-shaped silicon layer **106**; the second pillar-shaped silicon layer **109** formed on the second fin-shaped silicon layer **105**, the width of the first pillar-shaped silicon layer **110** being equal to the width of the first fin-shaped silicon layer **106** and the width of the second pillar-shaped silicon layer **109** being equal to the width of the second fin-shaped silicon layer **105**; the n-type diffusion layer **118** formed in an upper portion of the first fin-shaped silicon layer **106** and a lower portion of the first pillar-shaped silicon layer **110**; the n-type diffusion layer **115** formed in an upper portion of the first pillar-shaped silicon layer **110**; the p-type diffusion layer **125** formed in an upper portion of the second fin-shaped silicon layer **105** and a lower portion of the second pillar-shaped silicon layer **109**; the p-type diffusion layer **122** formed in an upper portion of the second pillar-shaped silicon layer **109**; the silicide **131** formed in upper portions of the n-type diffusion layer **118** and the p-type diffusion layer **125** in an upper portion of the first fin-shaped silicon layer **106** and in an upper portion of the second fin-shaped silicon layer **105**; the gate insulating film **126** formed around the first pillar-shaped silicon layer **110** and the first metal gate electrode **134***a* formed around the gate insulating film **126**; the gate insulating film **126** formed around the second pillar-shaped silicon layer **109** and the second metal gate electrode **134***b* formed around the gate insulating film **126**; the metal gate line **134***c* connected to the first metal gate electrode **134***a* and the second metal gate electrode **134***b* and extending in a direction perpendicular to the first fin-shaped silicon layer **106** and the second fin-shaped silicon layer **105**; and the first contact **144** formed on the n-type diffusion layer **115** formed in an upper portion of the first pillar-shaped silicon layer **110** and the second contact **143** formed on the p-type diffusion layer **122** formed in an upper portion of the second pillar-shaped silicon layer **109**, the first contact **144** being in direct contact with the n-type diffusion layer **115** formed in an upper portion of the first pillar-shaped silicon layer **110** and the second contact **143** being in direct contact with the p-type diffusion layer **122** formed in an upper portion of the second pillar-shaped silicon layer **109**.

As described above, it is possible to decrease a parasitic capacitance between a gate line and a substrate and provide a CMOS SGT manufacturing method for forming a nMOS SGT and a pMOS SGT from one dummy pattern using a gate-last process and provide a resulting SGT structure.

In the present invention, various embodiments and modifications can be made without deviating from the broad spirit and scope of the present invention. The above-described embodiment is illustrative of an example of the present invention, and does not limit the scope of the present invention.

In addition, it is apparent to persons skilled in the art that the technical scope of the present invention includes an embodiment where the conductivity types of p-type (including p+ type) and n-type (including n+ type) are reversed to those in the above description.

The invention claimed is:

1. A semiconductor device comprising:
- a first fin-shaped semiconductor layer on a substrate;
- a second fin-shaped semiconductor layer on the substrate;
- a first insulating film around the first fin-shaped semiconductor layer and the second fin-shaped semiconductor layer;
- a first pillar-shaped semiconductor layer on the first fin-shaped semiconductor layer;
- a second pillar-shaped semiconductor layer on the second fin-shaped semiconductor layer,
- wherein a width of a bottom of the first pillar-shaped semiconductor layer is equal to a width of a top of the first fin-shaped semiconductor layer and a width of a bottom of the second pillar-shaped semiconductor layer is equal to the width of a top of the second fin-shaped semiconductor layer;
- an n-type diffusion layer in an upper portion of the first fin-shaped semiconductor layer and a lower portion of the first pillar-shaped semiconductor layer;
- a p-type diffusion layer in an upper portion of the second fin-shaped semiconductor layer and a lower portion of the second pillar-shaped semiconductor layer;
- a first gate insulating film around the first pillar-shaped semiconductor layer;
- a first metal gate electrode around the first gate insulating film;
- a second gate insulating film around the second pillar-shaped semiconductor layer;
- a second metal gate electrode around the second gate insulating film; and
- a metal gate line connected to the first metal gate electrode and the second metal gate electrode and extending in a direction perpendicular to the first fin-shaped semiconductor layer and the second fin-shaped semiconductor layer.

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